SUZAKU-S
SZ130-U00
Hardware Manual

Version 1.0.2

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Table of Contents

List of Tables

List of Figures

1. Introduction

Thank you for your purchase of the SZ130-U00.

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This manual introduces the hardware specifications and the method to use the SZ130-U00.

We hope the information contained in this document will help you get the best functionality out of the SZ130-U00.

2. Precautions

2.1. Safety Precautions

Before using the SZ130-U00, please read the following safety precautions carefully to assure correct use.

This product uses semiconductor components designed for generic electronics equipment such as office automation equipment, communications equipment, measurement equipment and machine tools. Do not incorporate the product into devices such as medical equipment, traffic control systems, combustion control systems, safety equipment and so on which can directly threaten human life or pose a hazard to the body or property due to malfunction or failure. Moreover, products incorporating semiconductor components can be caused to malfunction or fail due to foreign noise or surge. To ensure there will be no risk to life, the body or property even in the event of malfunction or failure, be sure to take all possible measures in the safety system design, such as using protection circuits like limit switches or fuse breakers, or system multiplexing.

2.2. Operational Precautions

To avoid degradation, damage, malfunction or fire, the following safety precautions must be observed when handling the product.

- **Input Voltage**
  Do not attempt to apply input voltage higher than 3.3V+5%.
  Be careful about the polarity.

- **Interfaces**
  Do not connect signals other than specified to each interface (external I/O, RS-232C, Ethernet or JTAG).
  Use caution in polarity.
  Take care of input/output direction of signals.

- **Modification**
  Do not make modifications other than adding external I/O connectors or JTAG connectors (CON2, CON3, CON4, CON5 and CON7).

- **FPGA Programming**
  Be careful not to program the FPGA in a way that it can cause a collision of peripheral circuits (including onboard components) and a signal (i.e. output of the same signal from two devices).
  Use caution when programming the FPGA.

- **Power-on**
  Do not attempt to install or remove the FPGA I/O or JTAG connectors when power is applied to the board or peripheral circuits.

- **Static-Electricity**
  This board incorporates CMOS devices. Until using the board, store it in the provided antistatic package.

- **Latch-up**
  Due to excessive noise or a surge from the power supply or input/output, or sharp voltage fluctuations, the CMOS devices incorporated in the board can cause a latch-up. Once a latch-up occurs, this situation continues until the power supply is disconnected and thus can damage the devices. It is recommended to take safety measures such as adding a protection circuit to the noise-susceptible input/output line or not sharing a power supply with devices that can be the cause of noise.

- **Impact & Vibration**
  Guard against strong impact such as a drop or collision.
  Do not put this product on anything vibrating or rotating.
  Guard against strong vibration or centrifugal force.

- **High/Low Temperature & High Humidity**
  Do not use the product at locations subject to high/low temperatures and high humidity.

- **Dust**
  Do not use the product in dusty areas.

2.3. FPGA Precautions

- **FPGA Project Contained in This Product**
  The FPGA project and documentation contained in this product are provided “AS IS” without warranty of any kind including any warranty of merchantability or fitness for a particular purpose, reliability, correctness or accuracy. Furthermore, Atmark Techno, Inc. does not guarantee any outcomes resulting from the use of this product.
  This product uses vendor provided tools (Xilinx’s EDK/ISE or other vendor’s tools) and IP cores to build and compile FPGA projects and to create configuration data. Atmark Techno, Inc., however, does not distribute, support or guarantee these tools.

2.4. Software Precautions

- **Software Contained in this Product**
  The software and documentation contained in this product are provided “AS IS” without warranty of any kind including any warranty of merchantability or fitness for a particular purposes, reliability, correctness or accuracy. Furthermore, Atmark Techno, Inc. does not guarantee any outcomes resulting from the use of this product.

3. Getting Started

3.1. Preparation

Please make the following preparations before using the SZ130-U00.

- **Development PC**
  For hardware development, prepare a PC with one serial port and one parallel port that can run Windows2000 or WindowsXP.
  In addition, for software development, prepare a PC with one serial port that can run Linux.
  For more information about software development, refer to the associated Software Manual.

- **D-Sub9-pin Cross Cable**
  Prepare one cross cable for D-Sub9-pin (female-to-female) connection.

- **D-Sub9-pin to 10-pin Conversion Cable**
  Prepare one D-Sub9-pin to 10-pin conversion cable for connecting the D-Sub9-pin to the pin header (10-pin) on this board.

- **The Development Kit CD-ROM (hereafter called CD-ROM)**
  This development kit contains various manuals and source code relating to the SZ130-U00.

- **Serial Communication Software**
  Serial communication software such as minicom or Tera Term is required. (Linux software is included in the CD-ROM *(tools directory*).

- **DC3.3V Power Supply**
  Prepare one DC3.3V output power supply.

- **Xilinx ISE**
  Prepare Xilinx ISE8.1i or higher.
  For more information about Xilinx ISE, please contact a Xilinx distributor.

- **Xilinx EDK**
  Prepare Xilinx EDK8.1i or higher.
  For more information about Xilinx EDK, please contact a Xilinx distributor.

- **Xilinx Parallel Cable or Equivalent**
  Prepare one Xilinx Parallel Cable.
  For more information about this cable, please contact a Xilinx distributor.

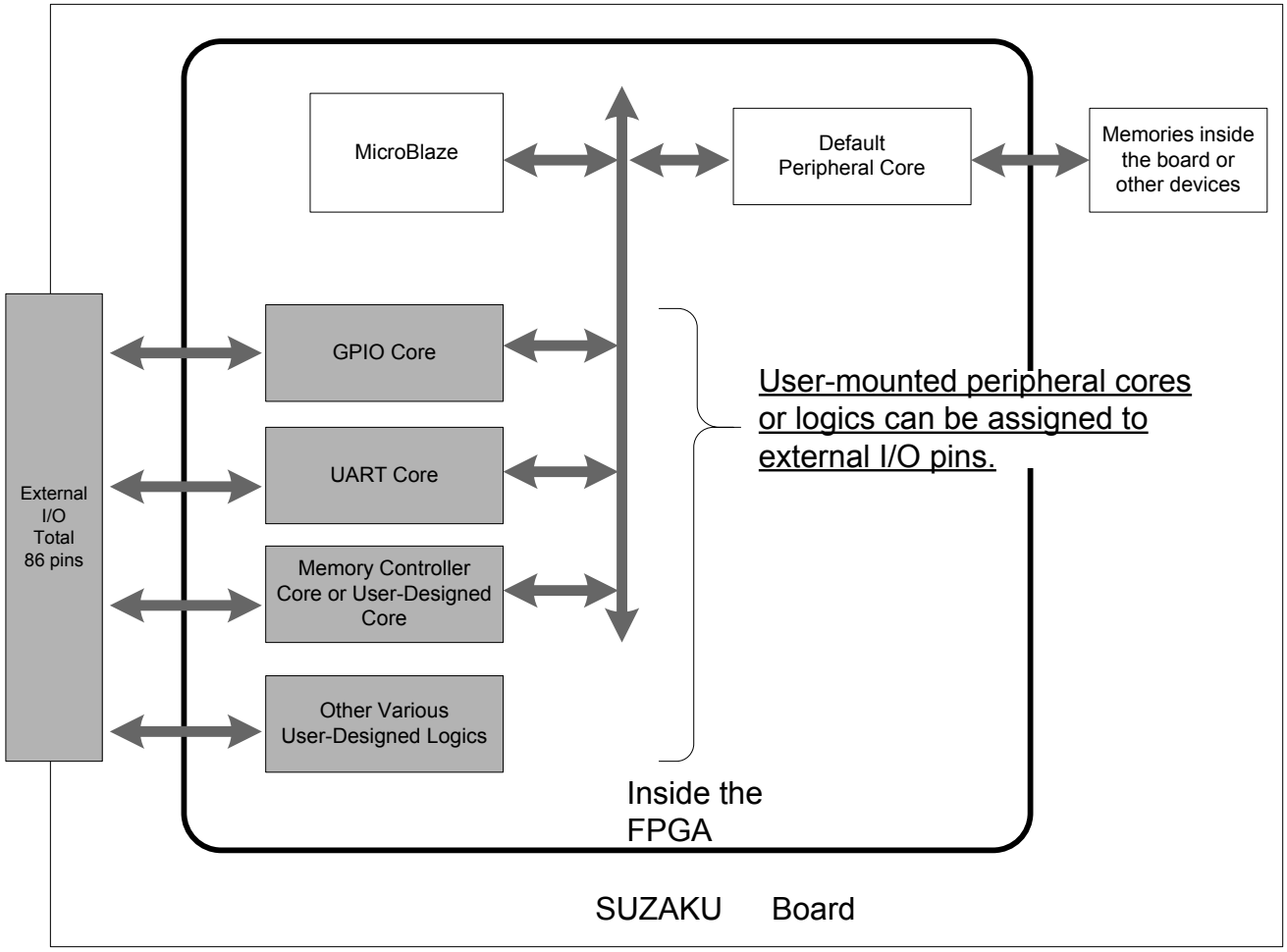
4. Overview

4.1. SZ130-U00 Features

The SZ130-U00 is a Xilinx's FPGA Spartan-3E based board computer.
It consists of a MicroBlaze soft processor and peripheral cores on the FPGA. It employs Linux (uCLinux) as an operating system.

- **Building the Soft P`rocessor and Peripheral Cores**
  The building of the MicroBlaze and peripheral cores utilizes Xilinx's EDK (Embedded Development Kit). The EDK enables the configuration of the MicroBlaze and peripheral cores in a GUI environment and automatically generates a netlist based on the configuration information.

- **Customization**
  The interior of the FPGA is designed for user-customization.
  The board is equipped with 86 external I/O pins that can be used at user's disposal.
  For instance, you can easily customize the board to increase the number of PIOs or UARTs by assigning these external I/O pins to them.



* To customize the FPGA, Xilinx's EDK and ISE are required. They can be obtained directly from Xilinx or through Xilinx's local distributor.

- **LAN**
  The board is equipped with a LAN (10Base-T/100Base-Tx) port for off-the-shelf LAN cable (UTP) connections.

- **Operating System**
  The board employs μCLinux as its standard operating system. It allows the use of a GNU assembler or C compiler in the development of application software.
  The board comes with a LAN control device driver and a variety of protocols for easy network configuration.
  For more information about operating system, refer to the Software Manual.

4.2. Specifications

The main specifications of this board are shown in Table 4-1.

Table 4-1 SZ130-U00 Specifications

FPGA		Xilinx Spartan-3E XC3S1200 FG320
Soft Processor		MicroBlaze
Crystal Oscillator		3.6864MHz (frequency multiplied by FPGA's internal DCM)
Memory	BRAM	504Kbits
	SDRAM	16Mbyte × 2
	SPI Flash	8Mbyte
Configuration		Stored in SPI Flash
JTAG		One port (FPGA)
SPI Flash Write		Dedicated pin
Ethernet		10Base-T/100Base-Tx
Serial		UART 115.2kbps
Timer		2ch (1ch is used by OS)
Free I/O Pin		86 pin
Reset Function		Software Reset
Power Supply		Power supply: 3.3V±3% Consumption current: 350mA typ (when processor is active)
Ambient Temperature		0 to 60 degrees C
Dimensions		72×47mm

4.3. Block Diagram

The entire block diagram of the SZ130-U00 is shown in Figure 4-1.
This is the minimum configuration that is needed to run uCLinux.

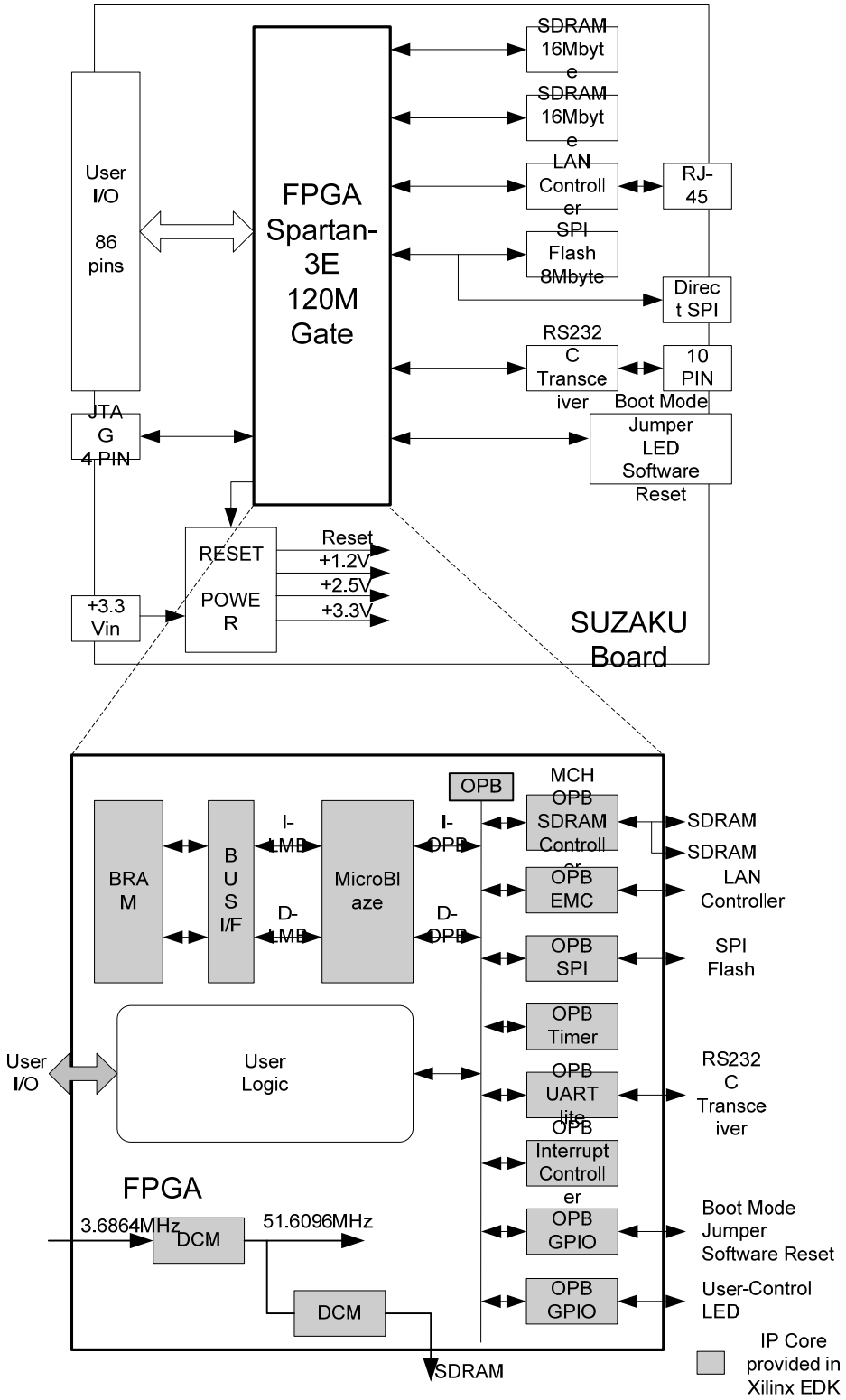


Figure 4-1 SZ130-U00 Block Diagram

4.4. Function

4.4.1. Processor

The board uses MicroBlaze in the FPGA. MicroBlaze has features listed below.

- 32-bit, RISC processor
- 32-bit , fixed length instruction
- 32 generic 32bit registers
- 3-stage pipeline
- Instruction cache and data cache
- Hardware multiplier
- Hardware debug logic supported

4.4.2. Bus

Bus consists of the following three types of buses.

- FPGA Internal LMB
  A dedicated bus used to connect MicroBlaze and BRAM (FPGA internal memory).
- FPGA Internal OPB
  A bus used to connect multiple peripheral IP cores.
  Customization is implemented by way of adding one or more peripheral cores to this bus.
- FPGA External bus
  A bus used to connect external memory devices via OPB EMC and OPB SDRAM.

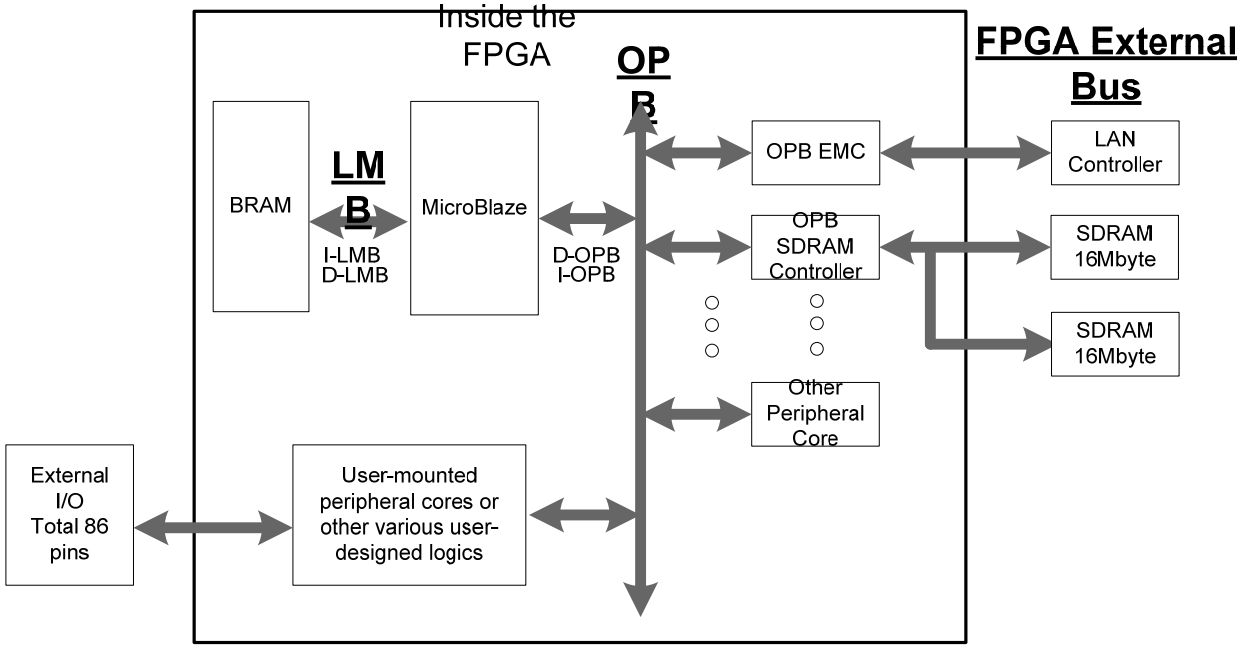


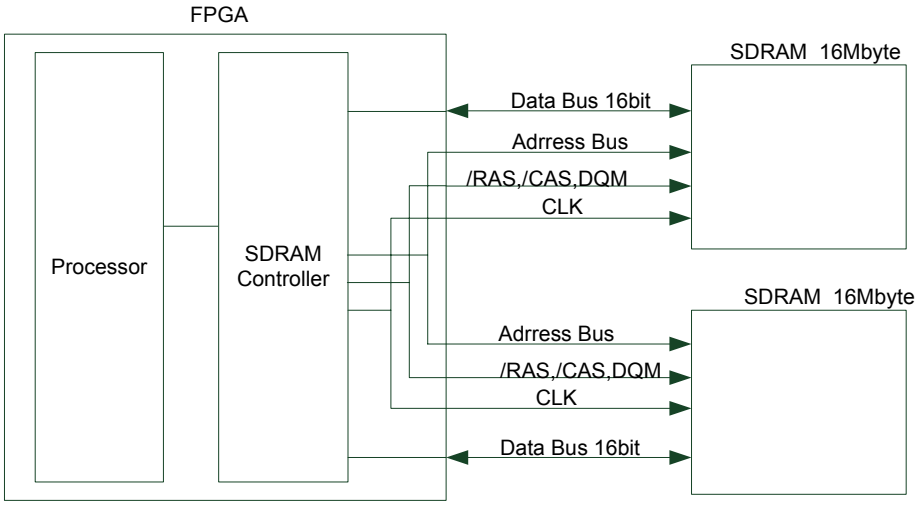
Figure 4-2 SZ130-U00 Bus Structure

4.4.3. Memory

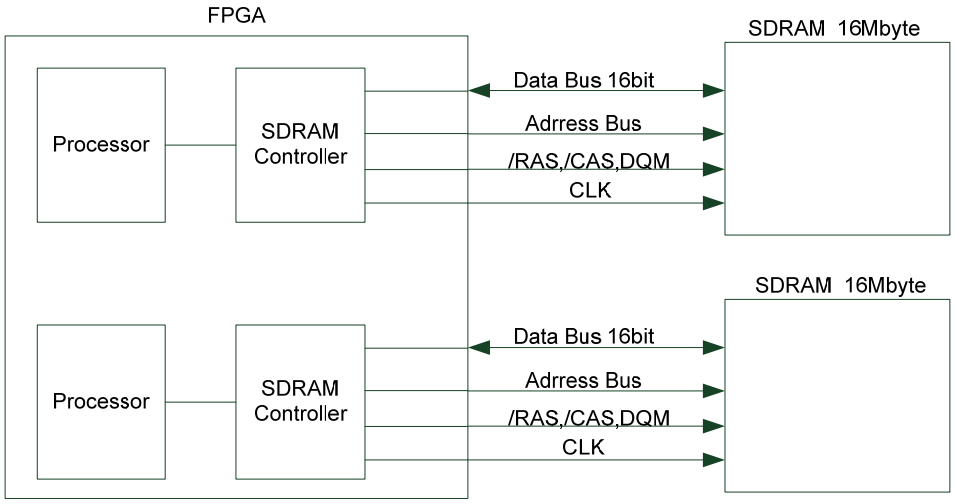
Memory consists of the following three types of memories.

・FPGA Internal BRAM (default 8KByte)
This memory is used for boot-programming.
After booting, this memory can be used for user programming except for the first 32-byte area (interrupt vector area).
・FPGA Internal SPI Flash memory
This 8MByte memory is used to store data such as high performance boot loader, Linux system and FPGA configuration.
The memory is connected to OPB via OPB SPI.
・FPGA External SDRAM 16MByte (* 2)
This memory is used as the main memory for Linux.
The memory is connected to OPB via OPB SDRAM.
Two SDRAM signal lines are completed separated with each other and connected to FPGA respectively.
For example, this allows the following application dependent on FPGA programming.

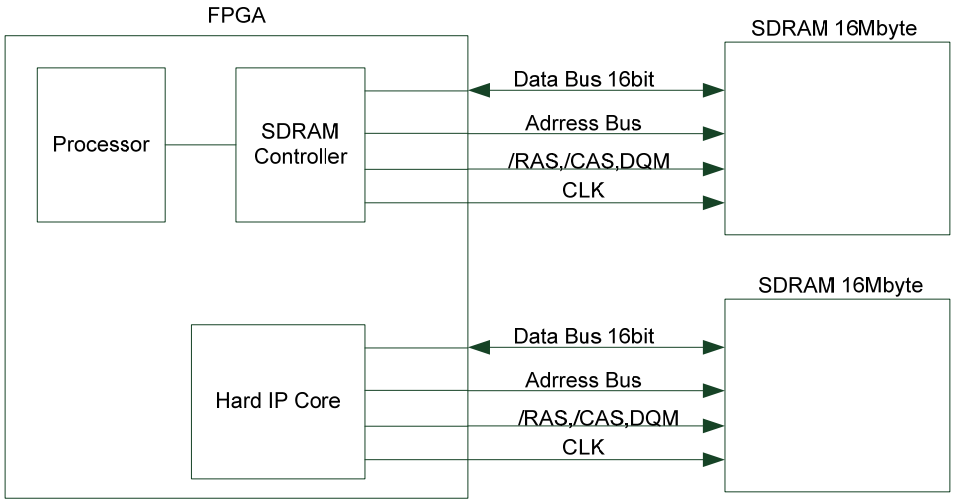
SUZAKU default single processor 32Mbyte Data32bit width



Processor 16Mbyte Data16bit width + Processor 16Mbyte Data16bit width



Processor 16Mbyte Data16bit width + Hard IP Core



4.4.4. Interrupt

The board uses OPB INTC in the FPGA as an OS interrupt controller.

4.4.5. Timer

The board uses OPB Timer in the FPGA as an OS timer.

4.4.6. Serial Console

The board uses OPB UART Lite in the FPGA as an OS serial console.
OPB UART Lite is connected to the CON1 connector via a RS-232C transceiver.
The RS-232C transceiver is the 4-channel version. The first two channels are used for the OS serial console and the remaining two channels are unused. Using these unused channels, you can connect GPIO or user logic for flow control, or connect another OPB UART Lite as the second UART port.

Serial console setting:

Transfer rate:	115.2kbps
Data:	8bit
Stop Bit:	1bit
Flow Control:	None

4.4.7. LAN

The LAN controller uses SMSC's LAN9115 outside FPGA.
The LAN9115 is connected to OPB via OPB EMC.
The LAN controller is equipped with a RJ-45 connector for connection of a generic LAN cable (UTP).

4.4.8. External I/O

The board provides 86 external pins that can be used at user's disposal (CON2, CON3, CON4 and CON5). (Note: connectors are not installed).
All external I/Os are directly connected to FPGA's free I/O pins.
The power for FPGA I/Os is supplied from the internal logic power supply +3.3V.
For rated value of I/O voltage and driving current, refer to the Spartan-3E data sheet.

Due to the sequence and delay circuits, the internal logic power supply +3.3V takes up to 20msec for startup. To avoid a latch-up, all devices connecting to external I/Os must use the internal logic power output +3.3V on this board (refer to Section 4.4.15 "Internal Logic Power Output +3.3V), otherwise a buffer device will be required.

4.4.9. FPGA Configuration

The on-board SPI Flash memory is used to store the FPGA configuration data. The current flash memory chip on SUZAKU is ST Microelectronics's M25P64 [1].

Configuration data can be written to the flash memory with the SPI Writer software tool included in the SUZAKU Starter Kit CD-ROM.

SPI Writer stores the configuration data in the first 1MB region of the SPI flash memory and the FPGA will then read that region when it needs to be configured.

The SPI flash memory is also used to store software data such as the Linux kernel, device drivers, applications, and configuration data. The region below the first 1MB region is reserved for this software use.

While Xilinx also offers a similar configuration tool named xspi, it erases the entire flash memory including the region reserved for software on SUZAKU. The use of xspi may therefore be problematic if you intend to use software on SUZAKU. Therefore we recommend the use of SPI Writer unless you fully understand the implications of using xspi.

The SUZAKU Starter Kit Guide makes use of SPI Writer in the following chapters.

[1] This is subject to change without prior notice.

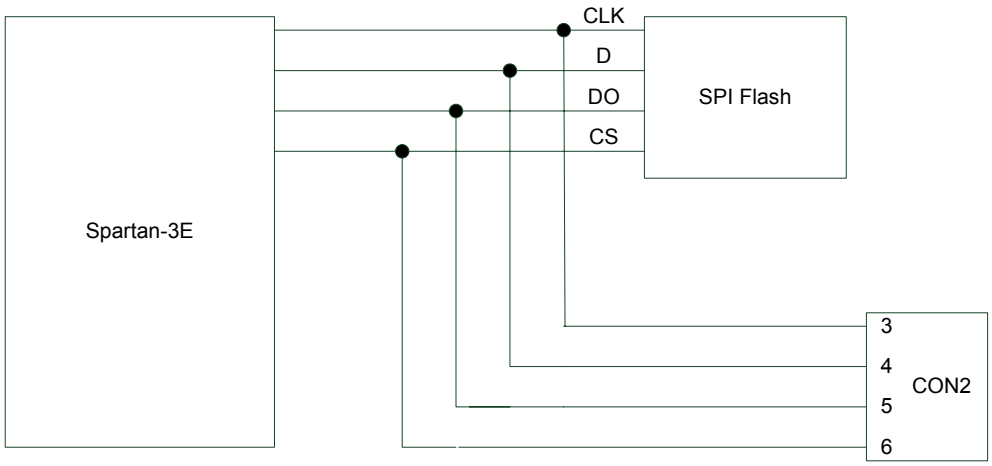
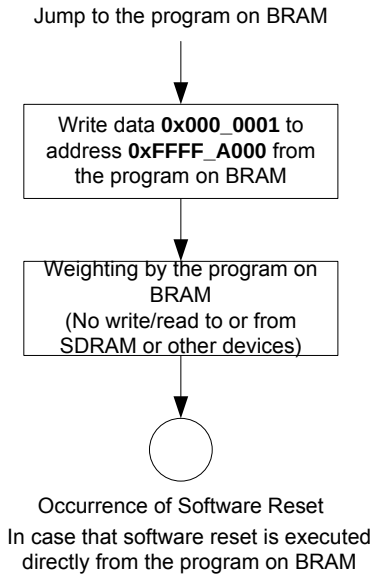


Figure 4-3 FPGA Configuration

4.4.10. Software Reset Function

When software reset is executed, the board again reads the configuration data from the Flash memory. It then executes FPGA configuration and outputs the reset signal to each device IC.
This software reset can be executed either by using a Linux reboot command or writing the data, 0x0000_0001, to the address 0xFFFF_A000 directly from a program on BRAM. If the software reset is executed directly from a program on BRAM, be careful not to write or read to or from SDRAM or other devices (including execution of a program).



4.4.11. JTAG

- JTAG connector for FPGA (CON7)

This is a JTAG connector for FPGA (not mounted).
It is directly connected to the JTAG-pin on FPGA.
The I/O voltage of this JTAG is +2.5V. Please use a JTAG cable compatible with +2.5V output.
TMS, TDI and TCK are all pulled up to +2.5V in the board via 4.7kΩ.

4.4.12. Jumpers

The following two types of jumpers are provided.

- **Boot Mode Jumper (JP1) – connected to F5 of Spartan-3E の F5**

This jumper is used to switch the boot mode.
When it is set to “open”, the board will boot in auto mode.
When it is set to “short”, the board will go into boot loader mode.
(For more information about boot mode, refer to the associated Software Manual).

- **FPGA Programming Jumper (JP2) – connected to T3 INIT_B of Spartan-3E)**

This jumper is used to program the SPI Flash memory.
When it is set to “open”, the board will boot in normal mode.
(When this jumper is shorted at power-on, FPGA configuration will be halted to allow programming to the SPI Flash memory).

4.4.13. LEDs

The board provides the following two types of LEDs.

- **Power-on LED Green (D3)**

This LED will light when 3.3V is supplied to the board.

- **User-Control LED Red (D1) – connected to T3 INIT_B of Spartan-3E**

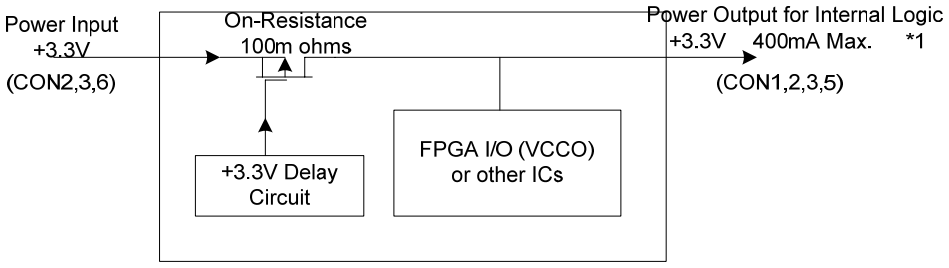
This LED is user-controllable.
It will light at “LO” level.
It is connected to the FPGA.

4.4.14. Power Input +3.3V

Power can be fed to the board from the “+3.3V Power Input” at CON2, CON3 and CON6.
The +3.3V must be ±3% in accuracy and simple increment.
Do not attempt to repeatedly turn the board on-and-off at very short time intervals.
The input is equipped with laminated ceramic condenser 22μF.

4.4.15. Internal Logic Power Output +3.3V

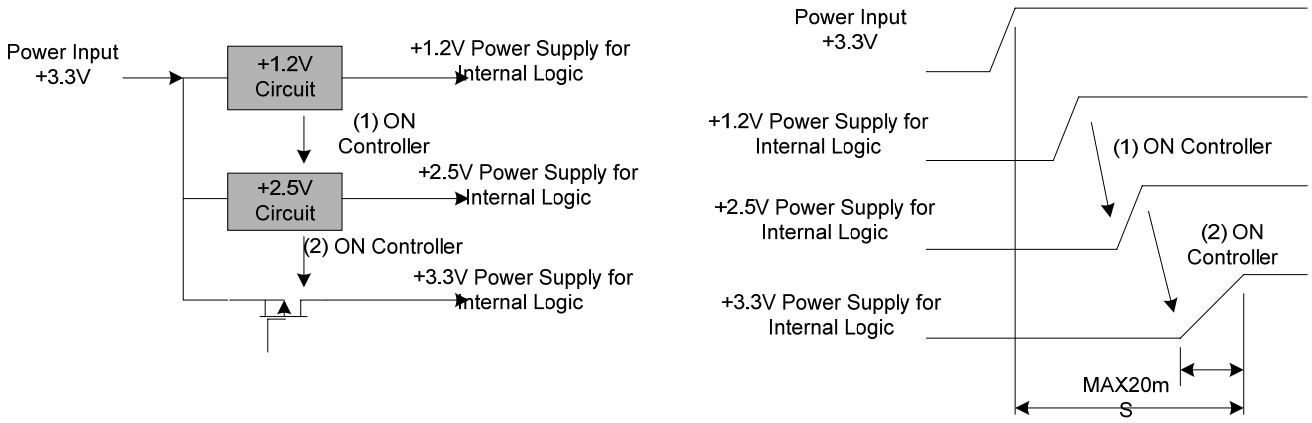
The internal logic power output +3.3V is a power supply used to feed +3.3V to I/O(VCCO) on FPGA and other ICs.
Up to 400mA [*1] can be supplied to the external devices from CON1, CON2, CON3 and CON5. However, due to significantly large load variation on the external devices, voltage variation can occur dependent on the response of the power input +3.3V.



*1: If signals are sent from the external I/O, total maximum current is given by:
Total Maximum Current = 400mA — Output Current of External I/O Signal

4.4.16. Internal Power Supply Sequence

The internal power supply will boot up in the following sequence.



5. Memory Map

5.1. SZ130-U00 Memory Map

The memory map of the board is shown in Table 5-1.
It is the minimum configuration required to run uCLinux.

Table 5-1 SZ130-U00 Memory Map

Start Address	End Address	Peripheral	Device
0x0000 0000	0x0000 1FFF	BRAM	
0x0000 1000	0x7FFF FFFF	Reserved	
0x8000 0000	0x80FF FFFF	OPB-SDRAM Controller	SDRAM 16MByte
0x8100 0000	0xFEFF FFFF	Free	
0xFF00 0000	0xFF7F FFFF	OPB-SPI	SPI Flash Memory 8MByte
0xFF80 0000	0xFFCF FFFF	Free	
0xFFE0 0000	0xFFEF FFFF	OPB-EMC	LAN Controller
0xFFF0 0000	0xFFFF 0FFF	Free	
0xFFFF 1000	0xFFFF 10FF	OPB-Timer	
0xFFFF 1100	0xFFFF 1FFF	Free	
0xFFFF 2000	0xFFFF 20FF	OPB-UART Lite	RS-232C
0xFFFF 2100	0xFFFF 2FFF	Free	
0xFFFF 3000	0xFFFF 30FF	OPB-Interrupt Controller	
0xFFFF 3100	0xFFFF 9FFF	Free	
0xFFFF A000	0xFFFF A1FF	OPB-GPIO	Boot Mode Jumper Software Reset
0xFFFF A200	0xFFFF A3FF	OPB-GPIO	LED
0xFFFF A400	0xFFFF FFFF	Free	

6. FPGA Pin Assignment

The following tables show all pin assignments of the FPGA (Xilinx Spartan-3E XC3S1200E FG320).

Table 6-1 FPGA Pin Assignment – External I/O (1/3)

No.	Bank	Signal Name	I/O	Function	Connected to
B11	0	IOh_0	I/O	External I/O	(See Section 7)
A11	0	IOc_0	I/O	External I/O	(See Section 7)
A16	0	IO_L01N_0	I/O	External I/O	(See Section 7)
B16	0	IO_L01P_0	I/O	External I/O	(See Section 7)
C14	0	IO_L03N_0	I/O	External I/O	(See Section 7)
D14	0	IO_L03P_0	I/O	External I/O	(See Section 7)
A14	0	IO_L04N_0	I/O	External I/O	(See Section 7)
B14	0	IO_L04P_0	I/O	External I/O	(See Section 7)
E12	0	IO_L06N_0	I/O	External I/O	(See Section 7)
F12	0	IO_L06P_0	I/O	External I/O	(See Section 7)
F11	0	IO_L08N_0	I/O	External I/O	(See Section 7)
E11	0	IO_L08P_0	I/O	External I/O	(See Section 7)
D11	0	IO_L09N_0	I/O	External I/O	(See Section 7)
C11	0	IO_L09P_0	I/O	External I/O	(See Section 7)
E10	0	IO_L11N_0/GCLK5	I/O	External I/O	(See Section 7)
D10	0	IO_L11P_0/GCLK4	I/O	External I/O	(See Section 7)
A10	0	IO_L12N_0	I/O	External I/O	(See Section 7)
B10	0	IO_L12P_0	I/O	External I/O	(See Section 7)
D9	0	IO_L14N_0/GCLK11	I/O	External I/O	(See Section 7)
C9	0	IO_L14P_0/GCLK10	I/O	External I/O	(See Section 7)
F9	0	IO_L15N_0	I/O	External I/O	(See Section 7)
E9	0	IO_L15P_0	I/O	External I/O	(See Section 7)
T17	1	IO_L01N_1	I/O	External I/O	(See Section 7)
U18	1	IO_L01P_1	I/O	External I/O	(See Section 7)
T18	1	IO_L02N_1	I/O	External I/O	(See Section 7)
R18	1	IO_L02P_1	I/O	External I/O	(See Section 7)
R16	1	IO_L03N_1	I/O	External I/O	(See Section 7)
R15	1	IO_L03P_1	I/O	External I/O	(See Section 7)
M13	1	IO_L05N_1	I/O	External I/O	(See Section 7)
M14	1	IO_L05P_1	I/O	External I/O	(See Section 7)
P18	1	IO_L06N_1	I/O	External I/O	(See Section 7)
P17	1	IO_L06P_1	I/O	External I/O	(See Section 7)

Table 6-2 FPGA Pin Assignment – External I/O (2/3)

No.	Bank	Signal Name	I/O	Function	Connected to
M16	1	IO_L07P_1	I/O	External I/O	(See Section 7)
M15	1	IO_L07N_1	I/O	External I/O	(See Section 7)
M18	1	IO_L08N_1	I/O	External I/O	(See Section 7)
N18	1	IO_L08P_1	I/O	External I/O	(See Section 7)
L15	1	IO_L09N_1	I/O	External I/O	(See Section 7)
L16	1	IO_L09P_1	I/O	External I/O	(See Section 7)
L17	1	IO_L10N_1	I/O	External I/O	(See Section 7)
L18	1	IO_L10P_1	I/O	External I/O	(See Section 7)
K12	1	IO_L15P_1	I/O	External I/O	(See Section 7)
K13	1	IO_L11P_1	I/O	External I/O	(See Section 7)
K14	1	IO_L12N_1	I/O	External I/O	(See Section 7)
K15	1	IO_L12P_1	I/O	External I/O	(See Section 7)
J16	1	IO_L13N_1	I/O	External I/O	(See Section 7)
J17	1	IO_L13P_1	I/O	External I/O	(See Section 7)
J14	1	IO_L14N_1	I/O	External I/O	(See Section 7)
J15	1	IO_L14P_1	I/O	External I/O	(See Section 7)
J13	1	IO_L15N_1	I/O	External I/O	(See Section 7)
J12	1	IO_L15P_1	I/O	External I/O	(See Section 7)
H17	1	IO_L16N_1	I/O	External I/O	(See Section 7)
H16	1	IO_L16P_1	I/O	External I/O	(See Section 7)
H15	1	IO_L17N_1	I/O	External I/O	(See Section 7)
H14	1	IO_L17P_1	I/O	External I/O	(See Section 7)
G16	1	IO_L18N_1	I/O	External I/O	(See Section 7)
G15	1	IO_L18P_1	I/O	External I/O	(See Section 7)
F17	1	IO_L19N_1	I/O	External I/O	(See Section 7)
F18	1	IO_L19P_1	I/O	External I/O	(See Section 7)
G13	1	IO_L20N_1	I/O	External I/O	(See Section 7)
G14	1	IO_L20P_1	I/O	External I/O	(See Section 7)
F14	1	IO_L21N_1	I/O	External I/O	(See Section 7)
F15	1	IO_L21P_1	I/O	External I/O	(See Section 7)
D16	1	IO_L23N_1	I/O	External I/O	(See Section 7)
D17	1	IO_L23P_1	I/O	External I/O	(See Section 7)
C17	1	IO_L24N_1	I/O	External I/O	(See Section 7)
C18	1	IO_L24P_1	I/O	External I/O	(See Section 7)

Table 6-3 FPGA Pin Assignment – External I/O (3/3)

No.	Bank	Signal Name	I/O	Function	Connected to
T15	2	IOf_2	I/O	External I/O	(See Section 7)
R14	2	IO_L24N_2	I/O	External I/O	(See Section 7)
J2	3	IO_L12N_3	I/O	External I/O	(See Section 7)
J1	3	IO_L12P_3	I/O	External I/O	(See Section 7)
K4	3	IO_L13N_3	I/O	External I/O	(See Section 7)
K3	3	IO_L13P_3	I/O	External I/O	(See Section 7)
K5	3	IO_L14N_3	I/O	External I/O	(See Section 7)
K6	3	IO_L14P_3	I/O	External I/O	(See Section 7)
L2	3	IO_L15N_3	I/O	External I/O	(See Section 7)
L1	3	IO_L15P_3	I/O	External I/O	(See Section 7)
L4	3	IO_L16N_3	I/O	External I/O	(See Section 7)
L3	3	IO_L16P_3	I/O	External I/O	(See Section 7)
L5	3	IO_L17N_3	I/O	External I/O	(See Section 7)
L6	3	IO_L17P_3	I/O	External I/O	(See Section 7)
M3	3	IO_L18N_3	I/O	External I/O	(See Section 7)
M4	3	IO_L18P_3	I/O	External I/O	(See Section 7)
M6	3	IO_L19N_3	I/O	External I/O	(See Section 7)
M5	3	IO_L19P_3	I/O	External I/O	(See Section 7)
N5	3	IO_L20N_3	I/O	External I/O	(See Section 7)
N4	3	IO_L20P_3	I/O	External I/O	(See Section 7)

Table 6-4 FPGA Pin Assignment – Internal Device (1/3)

No.	Bank	Signal Name	I/O	Function	Connected to
A7	0	SD1_DQML	O	SDRAM QDML	SDRAM #1
A8	0	SD0_DQ0	I/O	SDRAM Data Bus	SDRAM #0
C4	0	SD0_DQ8	I/O	SDRAM Data Bus	SDRAM #0
D13	0	SD1_A4	O	SDRAM Address Bus	SDRAM #1
E13	0	FPGA_RESET_EN	O	Self-Reset Output	Reset Circuit
G9	0	SD0_DQ15	I/O	SDRAM Data Bus	SDRAM #0
B13	0	CNSL_RTS	O	Console RTS	RS-232C Transceiver =>CON1
A13	0	CNSL_TXD	O	Console TXD	RS-232C Transceiver =>CON1
F8	0	SD0_DQ1	I/O	SDRAM Data Bus	SDRAM #0
E8	0	SD0_DQ14	I/O	SDRAM Data Bus	SDRAM #0
D7	0	SD0_DQ2	I/O	SDRAM Data Bus	SDRAM #0
C7	0	SD0_DQ13	I/O	SDRAM Data Bus	SDRAM #0
E7	0	SD0_DQ12	I/O	SDRAM Data Bus	SDRAM #0
F7	0	SD0_DQ3	I/O	SDRAM Data Bus	SDRAM #0
A6	0	SD0_DQ11	I/O	SDRAM Data Bus	SDRAM #0
B6	0	SD0_DQ4	I/O	SDRAM Data Bus	SDRAM #0
E6	0	SD1_WEb	O	SDRAM WE*	SDRAM #1
D6	0	SD1_DQMH	O	SDRAM QDMH	SDRAM #1
D5	0	SD0_DQ6	I/O	SDRAM Data Bus	SDRAM #0
C5	0	SD0_DQ10	I/O	SDRAM Data Bus	SDRAM #0
B4	0	SD0_DQ5	I/O	SDRAM Data Bus	SDRAM #0
A4	0	SD0_DQ9	I/O	SDRAM Data Bus	SDRAM #0
B3	0	SD1_CASb	O	SDRAM CAS*	SDRAM #1
C3	0	SD0_DQ7	I/O	SDRAM Data Bus	SDRAM #0
A12	0	CSb	O	LAN9115 CS*	LAN9115
D12	0	CNSL_CTS	I	Console CTS	RS-232C Transceiver =>CON1
C12	0	CNSL_RXD	I	Console RXD	RS-232C Transceiver =>CON1
B9	0	SD0_CLK	I	SDRAM Clock DCM Feedback Input	SDRAM #0
B8	0	SD1_CLK	I	SDRAM Clock DCM Feedback Input	SDRAM #1
P16	1	SD1_A6	O	SDRAM Address Bus	SDRAM #1
N14	1	SD1_A1	O	SDRAM Address Bus	SDRAM #1
N15	1	SD1_A5	O	SDRAM Address Bus	SDRAM #1
E16	1	SD1_A2	O	SDRAM Address Bus	SDRAM #1
E15	1	SD1_A3	O	SDRAM Address Bus	SDRAM #1

Table 6-5 FPGA Pin Assignment – Internal Device (2/3)

No.	Bank	Signal Name	I/O	Function	Connected to
P9	2	D12	I/O	LAN9115 Data Bus	LAN9115
R11	2	D7	I/O	LAN9115 Data Bus	LAN9115
U6	2	SD1_DQ13	I/O	SDRAM Data Bus	SDRAM #1
U13	2	SD1_A8	O	LAN9115 Address Bus	SDRAM #1
V7	2	SD1_DQ7	I/O	SDRAM Data Bus	SDRAM #1
R9	2	D13	I/O	LAN9115 Data Bus	LAN9115
V11	2	SD1_BA0	O	SDRAM BA0	SDRAM #1
U5	2	SD1_DQ15	I/O	SDRAM Data Bus	SDRAM #1
T3	2	IO_L01N_2/INIT_B	I/O	INTT_B User-Control LED	
U3	2	FR_CSb	O	SPI Flash CS*	
T4	2	FR_D	O	SPI Flash Data In	
U4	2	SD1_DQ9	I/O	SDRAM Data Bus	SDRAM #1
T5	2	SD1_DQ4	I/O	SDRAM Data Bus	SDRAM #1
R5	2	A7	O	LAN9115 Address Bus	LAN9115
P6	2	A5	O	LAN9115 Address Bus	LAN9115
R6	2	A6	O	LAN9115 Address Bus	LAN9115
V6	2	SD1_DQ6	I/O	SDRAM Data Bus	SDRAM #1
V5	2	SD1_DQ5	I/O	SDRAM Data Bus	SDRAM #1
P7	2	A4	O	LAN9115 Address Bus	LAN9115
N7	2	A3	O	LAN9115 Address Bus	LAN9115
N8	2	D15	I/O	LAN9115 Data Bus	LAN9115
P8	2	A1	O	LAN9115 Address Bus	LAN9115
T8	2	SD0_CLK	O	SDRAM Clock Output	SDRAM #0
R8	2	A2	O	LAN9115 Address Bus	LAN9115
M9	2	D10	I/O	LAN9115 Data Bus	LAN9115
N9	2	D11	I/O	LAN9115 Data Bus	LAN9115
V9	2	D14	I/O	LAN9115 Data Bus	LAN9115
U9	2	SD1_CLK	O	SDRAM Clock Output	SDRAM #1
P10	2	D8	I/O	LAN9115 Data Bus	LAN9115
R10	2	D9	I/O	LAN9115 Data Bus	LAN9115
N10	2	FR_DO	O	SPI Flash Data Out	
M10	2	SD1_BA1	O	SDRAM BA1	SDRAM #1
N11	2	D5	I/O	LAN9115 Data Bus	LAN9115
P11	2	D6	I/O	LAN9115 Data Bus	LAN9115
V13	2	D1	I/O	LAN9115 Data Bus	LAN9115
V12	2	D4	I/O	LAN9115 Data Bus	LAN9115
R12	2	D2	I/O	LAN9115 Data Bus	LAN9115
T12	2	D3	I/O	LAN9115 Data Bus	LAN9115
P12	2	SD1_A9	O	SDRAM Address Bus	SDRAM #1
N12	2	SD1_DQ8	I/O	SDRAM Data Bus	SDRAM #1
R13	2	D0	I/O	LAN9115 Data Bus	LAN9115
P13	2	WRb	O	LAN9115 WR*	LAN9115
T14	2	RDb	O	LAN9115 RD*	LAN9115

Table 6-6 FPGA Pin Assignment – Internal Device (3/3)

No.	Bank	Signal Name	I/O	Function	Connected to
U15	2	SD1_A7	O	SDRAM Address Bus	SDRAM #1
V15	2	SD1_A10	O	SDRAM Address Bus	SDRAM #1
U16	2	FR_CLK	O	SPI Flash Clock	
T16	2	SD1_A0	O	SDRAM Address Bus	SDRAM #1
U10	2	SYSCLK	I	System Clock Input	Oscillator 3.6864MHz
V14	2	IRQb	I	LAN9115 IRQ*	LAN9115
D4	3	SD1_RASb	O	SDRAM RAS*	SDRAM #1
C2	3	SD0_DQML	O	SDRAM DQML	SDRAM #0
C1	3	SD0_DQMH	O	SDRAM DQMH	SDRAM #0
D2	3	SD0_WEb	O	SDRAM WE*	SDRAM #0
D1	3	SD0_CASb	O	SDRAM CAS*	SDRAM #0
E1	3	SD0_A12	O	SDRAM Address Bus	SDRAM #0
E2	3	SD0_RASb	O	SDRAM RAS*	SDRAM #0
E3	3	SD1_A11	O	SDRAM Address Bus	SDRAM #0
E4	3	SD1_A12	O	SDRAM Address Bus	SDRAM #0
F2	3	SD0_A11	O	SDRAM Address Bus	SDRAM #0
F1	3	SD0_BA0	O	SDRAM BA0	SDRAM #0
G4	3	SD0_A8	O	SDRAM Address Bus	SDRAM #0
G3	3	SD0_A10	O	SDRAM Address Bus	SDRAM #0
G5	3	SD0_BA1	O	SDRAM BA1	SDRAM #0
G6	3	SD0_A9	O	SDRAM Address Bus	SDRAM #0
H5	3	SD0_A0	O	SDRAM Address Bus	SDRAM #0
H6	3	SD0_A7	O	SDRAM Address Bus	SDRAM #0
H3	3	SD0_A1	O	SDRAM Address Bus	SDRAM #0
H4	3	SD0_A6	O	SDRAM Address Bus	SDRAM #0
H1	3	SD0_A2	O	SDRAM Address Bus	SDRAM #0
H2	3	SD0_A5	O	SDRAM Address Bus	SDRAM #0
J4	3	SD0_A3	O	SDRAM Address Bus	SDRAM #0
J5	3	SD0_A4	O	SDRAM Address Bus	SDRAM #0
P1	3	SD1_DQ14	I/O	SDRAM Data Bus	SDRAM #1
P2	3	SD1_DQ3	I/O	SDRAM Data Bus	SDRAM #1
P4	3	SD1_DQ12	I/O	SDRAM Data Bus	SDRAM #1
P3	3	SD1_DQ11	I/O	SDRAM Data Bus	SDRAM #1
R2	3	SD1_DQ2	I/O	SDRAM Data Bus	SDRAM #1
R3	3	SD1_DQ10	I/O	SDRAM Data Bus	SDRAM #1
T1	3	SD1_DQ1	I/O	SDRAM Data Bus	SDRAM #1
T2	3	SD1_DQ0	I/O	SDRAM Data Bus	SDRAM #1
D3	3	RESET	I	System Reset Input	Reset Circuit
F5	3	JP_SET	I	Boot Mode Detect	JP1

Table 6-7 FPGA Pin Assignment – JTAG/Configuration

No.	Bank	Signal Name	I/O	Function	Connected to
B1		PROG_B PWR_RESETb	I	Configuration PROG_B	Reset Circuit
A17		TCK FPGA_TCK	O	JTAG	CON7
A2		TDI FPGA_TDI	O	JTAG	CON7
C16		TDO FPGA_TDO	I	JTAG	CON7
D15		TMS FPGA_TMS	O	JTAG	CON7
T10		CFG_M2	I	M2	Pull-up

The bit and byte labeling for the buses in the table above, such as LA(0 to 22), LD(0 to 15), and RAM_BS(0 to 1), is the same as the IBM POWER architecture. The most significant bit is number 0 and the least significant bit is 31.

7. Interface Specifications

7.1. Layout of Interfaces

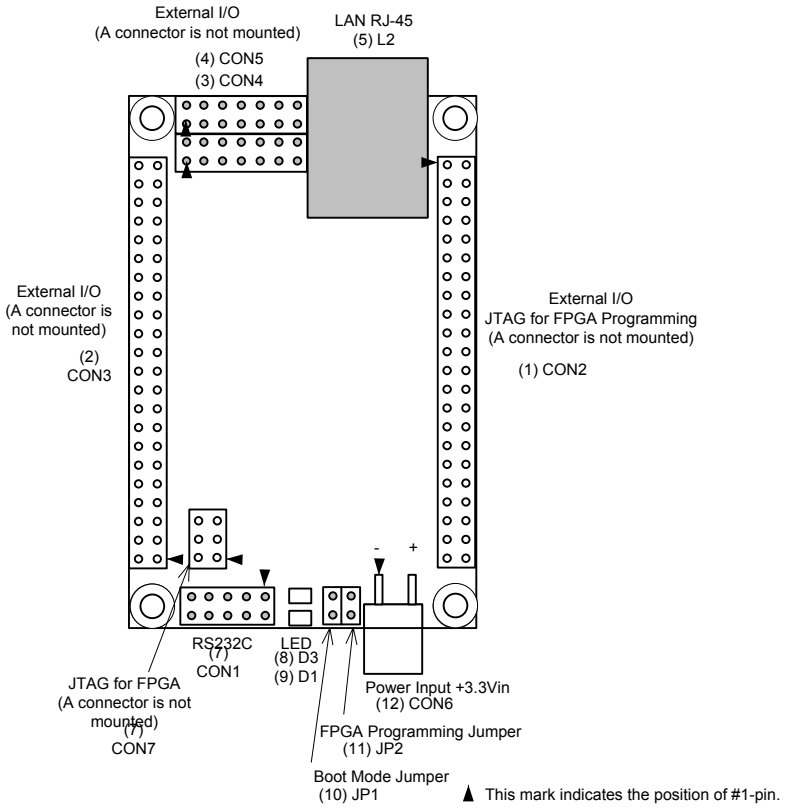


Figure 7-1 Layout of Interfaces

Table 7-1 Interface Details

	Part Number	Description
(1)	CON2	External I/O, JTAG connector for FPGA programming Total I/Os 32PIN
(2)	CON3	External I/O connector Total I/Os 34PIN
(3)	CON4	External I/O connector Total I/Os 10PIN
(4)	CON5	External I/O connector Total I/Os 10PIN
(5)	L2	Ethernet 10/100 Base-T connector
(6)	CON7	FPGA JTAG connector
(7)	CON1	RS-232C connector
(8)	D3	Power-on LED (Green)
(9)	D1	User Control LED (Red)
(10)	JP1	Boot mode jumper
(11)	JP2	Jumper for FPGA programming
(12)	CON6	Power input +3.3V connector

7.2. CON1 RS-232C

This RS-232C connector is connected to the FPGA via a level buffer. The type of the connector used on the board side and its maker name is A1-10PA-2.54DSA/Hirose (equivalent).

Table 7-2 Serial Console Setting

Item	Setting
Transfer Rate	115.2kbps
Data	8bit
Parity	None
Stop Bit	1bit
Flow Control	None

Table 7-3 CON1 RS-232C

No.	Signal Name	I/O	Function	
1			Unused	
2			Unused	
3	RXD	I	Spartan3E connection pin #	C12 (for serial console)
4	RTS	O	Spartan3E connection pin #	B13
5	TXD	O	Spartan3E connection pin #	A13 (for serial console)
6	CTS	I	Spartan3E connection pin #	D12
7			Unused	
8			Unused	
9	GND		Ground	
10	+3.3VOUT		Power output +3.3V for internal logic	

7.3. CON2 External I/O, SPI Flash Connector

This is a connector for external I/O and SPI Flash which connects to “CON2” of the LED/SW board.

Table 7-4 CON2 SPI Connector for External I/O, Flash

No.	Signal Name	I/O	Function	
1	GND		Ground	
2	+3.3VOUT		Power output +3.3V for internal logic	
3	CLK	I	SPI Flash programming	
4	D	I	SPI Flash programming	
5	DO	O	SPI Flash programming	
6	nCS	I	SPI Flash programming	
7	IO_L20N_3	I/O	External I/O Spartan3E connection pin#	N5
8	IO_L20P_3	I/O	External I/O Spartan3E connection pin#	N4
9	IO_L19N_3	I/O	External I/O Spartan3E connection pin#	M6
10	IO_L19P_3	I/O	External I/O Spartan3E connection pin#	M5
11	IO_L18N_3	I/O	External I/O Spartan3E connection pin#	M3
12	IO_L18P_3	I/O	External I/O Spartan3E connection pin#	M4
13	IO_L17N_3	I/O	External I/O Spartan3E connection pin#	L5
14	IO_L17P_3	I/O	External I/O Spartan3E connection pin#	L6
15	IO_L16N_3	I/O	External I/O Spartan3E connection pin#	L4
16	IO_L16P_3	I/O	External I/O Spartan3E connection pin#	L3
17	IO_L15N_3	I/O	External I/O Spartan3E connection pin#	L2
18	IO_L15P_3	I/O	External I/O Spartan3E connection pin#	L1
19	GND		Ground	
20	IO_L14P_0/GCLK10	I/O	External I/O Spartan3E connection pin#	C9
21	GND		Ground	
22	IO_L14N_0/GCLK11	I/O	External I/O Spartan3E connection pin#	D9
23	IO_L14N_3	I/O	External I/O Spartan3E connection pin#	K5
24	IO_L14P_3	I/O	External I/O Spartan3E connection pin#	K6
25	IO_L13N_3	I/O	External I/O Spartan3E connection pin#	K4
26	IO_L13P_3	I/O	External I/O Spartan3E connection pin#	K3
27	IO_L12N_3	I/O	External I/O Spartan3E connection pin#	J2
28	IO_L12P_3	I/O	External I/O Spartan3E connection pin#	J1
29	IO_L15N_0	I/O	External I/O Spartan3E connection pin#	F9
30	IO_L15P_0	I/O	External I/O Spartan3E connection pin#	E9
31	IO_L12N_0	I/O	External I/O Spartan3E connection pin#	A10
32	IO_L12P_0	I/O	External I/O Spartan3E connection pin#	B10
33	IO_L09N_0	I/O	External I/O Spartan3E connection pin#	D11
34	IO_L09P_0	I/O	External I/O Spartan3E connection pin#	C11
35	IO_L08N_0	I/O	External I/O Spartan3E connection pin#	F11
36	IO_L08P_0	I/O	External I/O Spartan3E connection pin#	E11
37	IO_L06N_0	I/O	External I/O Spartan3E connection pin#	E12
38	IO_L06P_0	I/O	External I/O Spartan3E connection pin#	F12
39	IOh_0	I/O	External I/O Spartan3E connection pin#	B11
40	IOc_0	I/O	External I/O Spartan3E connection pin#	A11
41	GND		Ground	
42	GND		Ground	
43	+3.3VIN		Power input +3.3V	
44	+3.3VIN		Power input +3.3V	

7.4. CON3 External I/O Connector

This is an external I/O connector which connects to “CON3” of the LED/SW board.

Table 7-5 CON3 SPI Connector for External I/O, Flash

No.	Signal Name	I/O	Function	
1	+3.3VIN		Power input +3.3V	
2	+3.3VIN		Power input +3.3V	
3	GND		Ground	
4	GND		Ground	
5	IO_L04P_0	I/O	External I/O Spartan3E connection pin#	B14
6	IO_L04N_0	I/O	External I/O Spartan3E connection pin#	A14
7	IO_L03P_0	I/O	External I/O Spartan3E connection pin#	D14
8	IO_L03N_0	I/O	External I/O Spartan3E connection pin#	C14
9	IO_L01P_0	I/O	External I/O Spartan3E connection pin#	B16
10	IO_L01N_0	I/O	External I/O Spartan3E connection pin#	A16
11	IO_L24P_1	I/O	External I/O Spartan3E connection pin#	C18
12	IO_L24N_1	I/O	External I/O Spartan3E connection pin#	C17
13	IO_L23P_1	I/O	External I/O Spartan3E connection pin#	D17
14	IO_L23N_1	I/O	External I/O Spartan3E connection pin#	D16
15	IO_L21P_1	I/O	External I/O Spartan3E connection pin#	F15
16	IO_L21N_1	I/O	External I/O Spartan3E connection pin#	F14
17	IO_L20P_1	I/O	External I/O Spartan3E connection pin#	G14
18	IO_L20N_1	I/O	External I/O Spartan3E connection pin#	G13
19	IO_L19P_1	I/O	External I/O Spartan3E connection pin#	F18
20	IO_L19N_1	I/O	External I/O Spartan3E connection pin#	F17
21	IO_L18P_1	I/O	External I/O Spartan3E connection pin#	G15
22	IO_L18N_1	I/O	External I/O Spartan3E connection pin#	G16
23	IO_L11N_0/GCLK5	I/O	External I/O Spartan3E connection pin#	E10
24	GND		Ground	
25	IO_L11P_0/GCLK4	I/O	External I/O Spartan3E connection pin#	D10
26	GND		Ground	
27	IO_L17P_1	I/O	External I/O Spartan3E connection pin#	H14
28	IO_L17N_1	I/O	External I/O Spartan3E connection pin#	H15
29	IO_L16P_1	I/O	External I/O Spartan3E connection pin#	H16
30	IO_L16N_1	I/O	External I/O Spartan3E connection pin#	H17
31	IO_L15P_1	I/O	External I/O Spartan3E connection pin#	J12
32	IO_L15N_1	I/O	External I/O Spartan3E connection pin#	J13
33	IO_L14P_1	I/O	External I/O Spartan3E connection pin#	J15
34	IO_L14N_1	I/O	External I/O Spartan3E connection pin#	J14
35	IO_L13P_1	I/O	External I/O Spartan3E connection pin#	J17
36	IO_L13N_1	I/O	External I/O Spartan3E connection pin#	J16
37	IO_L12P_1	I/O	External I/O Spartan3E connection pin#	K15
38	IO_L12N_1	I/O	External I/O Spartan3E connection pin#	K14
39	IO_L11P_1	I/O	External I/O Spartan3E connection pin#	K13
40	IO_L11N_1	I/O	External I/O Spartan3E connection pin#	K12
41	NC			
42	EXRESETb		Unused	
43	+3.3VOUT		Power output +3.3V for internal logic	
44	GND		Ground	

7.5. CON4 External I/O Connector

This is an external I/O connector. It is not mounted on the board.

Table 7-6 CON4 SPI Connector for External I/O, Flash

No.	Signal Name	I/O	Function	
1			Unused	
2			Unused	
3	IO_L10P_1	I/O	External I/O Spartan3E connection pin#	L18
4	IO_L10N_1	I/O	External I/O Spartan3E connection pin#	L17
5	IO_L09P_1	I/O	External I/O Spartan3E connection pin#	L16
6	IO_L09N_1	I/O	External I/O Spartan3E connection pin#	L15
7	IO_L08P_1	I/O	External I/O Spartan3E connection pin#	N18
8	IO_L08N_1	I/O	External I/O Spartan3E connection pin#	M18
9	IO_L07P_1	I/O	External I/O Spartan3E connection pin#	M16
10	IO_L07N_1	I/O	External I/O Spartan3E connection pin#	M15
11	IO_L06P_1	I/O	External I/O Spartan3E connection pin#	P17
12	IO_L06N_1	I/O	External I/O Spartan3E connection pin#	P18

7.6. CON5 External I/O Connector

This is an external I/O connector. It is not mounted on the board.

Table 7-7 CON5 External I/O Connector

No.	Signal Name	I/O	Function	
1	GND		Ground	
2	+3.3VOUT		Power output +3.3V for internal logic	
3	IO_L05P_1	I/O	External I/O Spartan3E connection pin#	M14
4	IO_L05N_1	I/O	External I/O Spartan3E connection pin#	M13
5	IO_L03P_1	I/O	External I/O Spartan3E connection pin#	R15
6	IO_L03N_1	I/O	External I/O Spartan3E connection pin#	R16
7	IO_L02P_1	I/O	External I/O Spartan3E connection pin#	R18
8	IO_L02N_1	I/O	External I/O Spartan3E connection pin#	T18
9	IO_L01P_1	I/O	External I/O Spartan3E connection pin#	U18
10	IO_L01N_1	I/O	External I/O Spartan3E connection pin#	T17
11	IOf_2	I/O	External I/O Spartan3E connection pin#	T15
12	IO_L24N_2	I/O	External I/O Spartan3E connection pin#	R14

7.7. CON6 Power Input +3.3V Connector

This is a power input connector. The power input +3.3V must be +3.3V±3% in simple increment.
It is connected to Power Input +3.3V of CON2 and CON3 in the board.
The type of a connector used on the board side and its maker name is B2PS-VH/JST Msg. (equivalent) and one used on the T-cable side is Housing VHR-2N/JST Msg. (equivalent) and Contact BVH-21T-P1.1/JST Msg. (equivalent) or BVH-41T-P1.1/JST Mfg. (equivalent).

7.8. CON7 FPGA JTAG Connector

This is a FPGA JTAG connector. The I/O voltage of JTAG is +2.5V. Please use a +2.5V-compatible JTAG connector.

Table 7-8 CON7 Spartan3E JTAG Connector

No.	Signal Name	I/O	Function
1	GND		Ground
2	+2.5VOUT		Power output +2.5V for internal logic
3	TCK	I	JTAG
4	TDI	I	JTAG
5	TDO	O	JTAG
6	TMS	I	JTAG

7.9. D1/D3 LEDs

These are User-control LED (Red) and Power-ON LED (Green).

Table 7-9 D1/D3 LED

Signal Name	I/O	Function
D1	O	User-control LED Spartan3E connection pin# T3
D3	O	This LED will light when 3.3V is supplied to the SUZAKU board.

7.10. JP1/JP2 Jumpers

These are jumpers used for boot mode setting and FPGA programming.

Table 7-10 JP1/JP2 Jumpers

Signal Name	I/O	Function
JP1	I	This is a jumper to select a boot mode. When it is set to "open", "auto-boot" is selected (When SUZAKU is started, Linux is automatically booted). When it is set to "short", "boot loader mode" is selected (this mode is used when only boot loader is started). In this manual, the jumper is set to "open".
JP2		This is a jumper used to program the configuration data to the Flash memory from the FPGA programming SPI. When it is set to "short", FPGA configuration data can be programmed into the Flash memory. (When this jumper is shorted, configuration can be stopped to the FPGA at the time of power-on and programming to the Flash memory is executed at this time).

7.11. SUZAKU L2 Ethernet 10/100Base-T

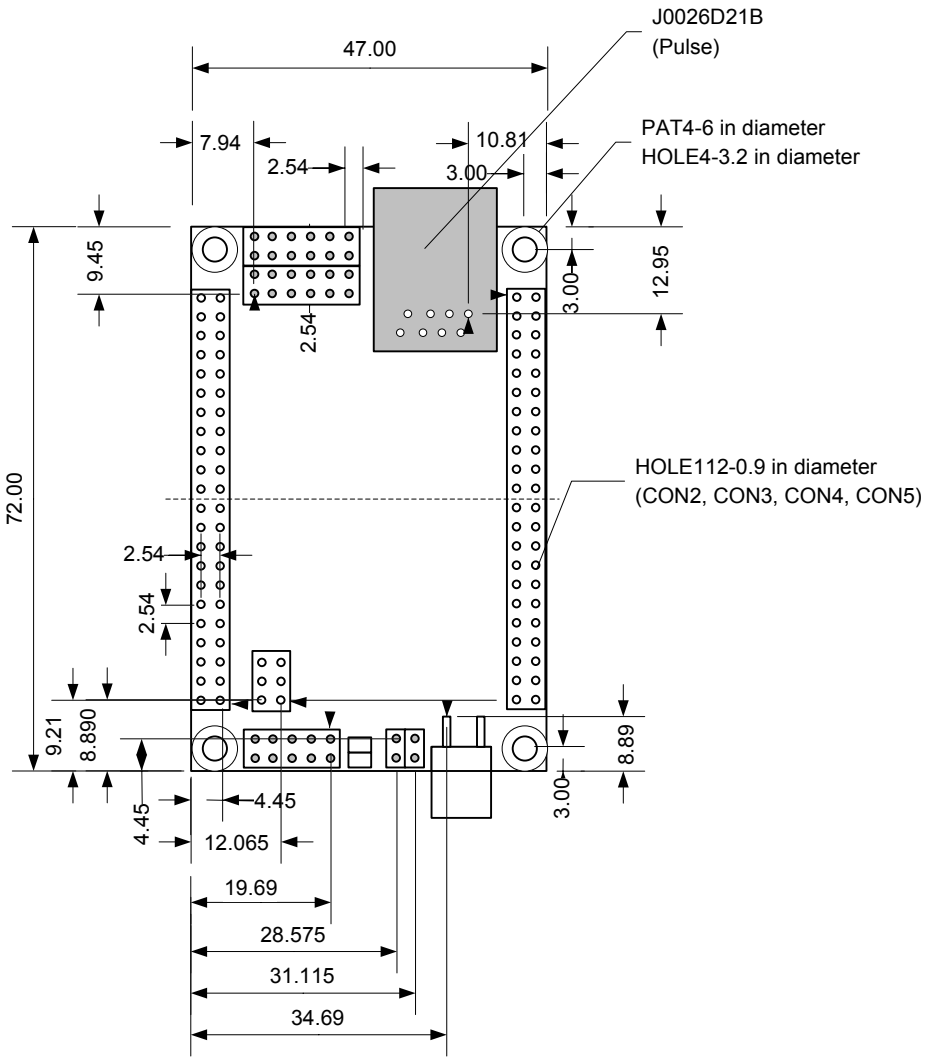
The type of the connector used on the board side and its maker name is J0026D21B/PULSE.

Table 7-11 L2 Ethernet 10/100 Base-T

No.	Signal Name	I/O	Function
1	TX+		Differential twist pair output+
2	TX-		Differential twist pair output-
3	RX+		Differential twist pair input+
4			75Ω termination (#4-pin and #5-pin are shorted)
5			75Ω termination (#4-pin and #5-pin are shorted)
6	RX-		Differential twist pair input-
7			75Ω termination (#7-pin and #8-pin are shorted)
8			75Ω termination (#7-pin and #8-pin are shorted)

8. Board Layout

The board layout is shown in Figure 8-1.



[Unit: mm]

Figure 8-1 SZ130-U00 Board Layout

Revision History

Revision	Revision Date	Description
1.0.0	July 14, 2006	Initial release
1.0.1	July 24, 2006	Corrected the pin assignment (9-pin and 10-pin of CON4)
1.0.2	August 11, 2006	Changed the spiwriter.zip directory path due to the change of CD-ROM content. Added “range of environmental temperature”

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