



AN010

Hardware Manual

Version 1.02

February 21, 2005

Atmark Techno, Inc.

<http://www.atmark-techno.com/>

Armadillo Official Site

<http://armadillo.atmark-techno.com/>

Table of Contents

| | | |
|---------|---|----|
| 1. | Introduction | 1 |
| 2. | Precautions | 2 |
| 2.1. | Safety Precautions | 2 |
| 2.2. | Operational Precautions | 2 |
| 2.3. | Software Precautions | 2 |
| 2.4. | Trademarks | 2 |
| 3. | Overview | 3 |
| 3.1. | Board Overview | 3 |
| 3.2. | Block Diagram | 4 |
| 4. | Memory Map | 5 |
| 4.1. | Physical Memory Map | 5 |
| 4.2. | Logical Memory Map When Using Linux | 6 |
| 5. | Interface Specifications | 7 |
| 5.1. | Interface Layout | 7 |
| 5.2. | CON1 (Serial Interface 1) | 8 |
| 5.3. | CON2 (Serial Interface 2) | 9 |
| 5.4. | CON3 (USB Interface) | 9 |
| 5.5. | CON4 (Parallel Interface) | 10 |
| 5.6. | CON5 (Parallel Interface) | 10 |
| 5.7. | CON6 (EP9315 JTAG) | 11 |
| 5.8. | CON7 | 11 |
| 5.9. | CON8 (Synchronous Serial / AC97 / I2S) | 12 |
| 5.10. | CON9 (IDE Interface) | 13 |
| 5.11. | CON10 (Compact Flash) | 14 |
| 5.12. | CON11 (LAN Connector) | 15 |
| 5.13. | CON12 (VGA Connector) | 15 |
| 5.14. | CON13 (Power Input Connector) | 16 |
| 5.15. | CON14 (Extension Power Input) | 16 |
| 5.16. | J1, J2 (PC/104-Compliant Extension Bus) | 17 |
| 5.16.1. | Precautions for PC/104 Extension Bus Access | 20 |
| 5.16.2. | Access Timing | 22 |
| 5.17. | LED (D4) | 23 |
| 5.18. | LED (D5, D6) | 23 |
| 5.19. | LED (D14) | 24 |
| 5.20. | JP1-2 | 24 |
| 5.20.1. | JP1 (Boot ROM Selection) | 24 |
| 5.20.2. | JP2 (Boot Linux Selection) | 24 |
| 5.21. | Connector Type | 25 |
| 5.22. | LED Types (Reference) | 25 |
| 6. | Other Functions | 26 |
| 6.1. | CPLD Internal Register (I/O Control Register) | 26 |
| 6.1.1. | Memory Map of I/O Control Register | 26 |
| 6.1.2. | Details of the I/O Control Registers | 27 |
| 6.1.3. | Structure of PC/104 Interrupt Controller | 28 |
| 6.2. | External Interrupts | 29 |
| 6.3. | LED (D1) | 29 |
| 6.4. | Calendar Clock (Real Time Clock) | 30 |
| 6.5. | Power Circuit | 30 |
| 7. | Board View | 31 |
| 8. | Revision History | 32 |

List of Tables

| | |
|--|----|
| Table 3-1 Armadillo-9 Board Specifications | 3 |
| Table 4-1 Physical Memory Map of Armadillo-9 | 5 |
| Table 4-2 Armadillo-9 Logical Memory Map When Using Linux | 6 |
| Table 5-1 Interface Details..... | 8 |
| Table 5-2 CON1 Signal Assignment | 8 |
| Table 5-3 CON2 Signal Assignment | 9 |
| Table 5-4 CON3 Signal Assignment | 9 |
| Table 5-5 CON4 Signal Assignment | 10 |
| Table 5-6 Electrical Specifications of CON4 Parallel Interface | 10 |
| Table 5-7 CON5 Signal Assignment | 10 |
| Table 5-8 CON8 Signal Assignment | 12 |
| Table 5-9 Pin Functionality in Each Mode | 12 |
| Table 5-10 CON9 Signal Assignment | 13 |
| Table 5-11 CON10 Signal Assignment | 14 |
| Table 5-12 CON11 Signal Assignment | 15 |
| Table 5-13 CON12 Signal Assignment | 15 |
| Table 5-14 Resolution and Horizontal Frequency..... | 15 |
| Table 5-15 CON13 Signal Assignment | 16 |
| Table 5-16 CON14 Signal Assignment | 16 |
| Table 5-17 J1 Signal Assignment (1)..... | 17 |
| Table 5-18 J1 Signal Assignment (2)..... | 18 |
| Table 5-19 J2 Signal Assignment (1)..... | 19 |
| Table 5-20 J2 Signal Assignment (2)..... | 19 |
| Table 5-21 Status of LED (D5, D6)..... | 23 |
| Table 5-22 Status of LED (D14)..... | 24 |
| Table 5-23 Jumper Settings and Function | 24 |
| Table 5-24 List of Connector Types | 25 |
| Table 5-25 LED Types | 25 |
| Table 6-1 Memory Map of I/O Control Register | 26 |
| Table 6-2 Details of I/O Control Registers | 27 |
| Table 6-3 Definition of Each Bit of I/O Control Registers | 27 |

List of Figures

| | |
|---|----|
| Figure 3-1 Block Diagram of Armadillo-9..... | 4 |
| Figure 5-1 Interface Layout | 7 |
| Figure 5-2 Memory Space of PC/104 Bus | 20 |
| Figure 5-3 Method to Access PC/104 Bus | 21 |
| Figure 5-4 PC/104 Bus Access Timing | 22 |
| Figure 5-5 LED (D4) Connections | 23 |
| Figure 5-6 LED (D5, 6) Connections | 23 |
| Figure 5-7 LED(D14) Connections | 24 |
| Figure 5-8 Jumper Connector | 25 |
| Figure 6-1 Structure of PC/104 Interrupt Controller | 28 |
| Figure 6-2 EXTIRQ Connections..... | 29 |
| Figure 6-3 LED (D1) Connections | 29 |
| Figure 6-4 Connection of CPU (EP9315) and RTC | 30 |
| Figure 6-5 Armadillo-9 Power Circuit..... | 30 |
| Figure 7-1 Armadillo-9 Board View..... | 31 |

1. Introduction

Thank you for your purchase of the Armadillo-9.

The Armadillo-9 is a small single board computer that uses an ARM9 processor (Cirrus Logic EP9315: 200MHz). It is equipped with 100Mbps network functionality as well as a wide range of interfaces including serial, USB, IDE and VGA. The Compact Flash slot allows for connection of I/O cards such as memory storage, PHS cards and wireless LAN cards. Also, the PC/104 bus enables functional expansion.

As the Armadillo-9 employs Linux as its standard operating system, you will be able to take advantage of the rich array of open-source software resources. Software development can be carried out using the GNU assembler, C-compiler and so on.



This manual covers the hardware specifications and methods of use of the Armadillo-9. We hope the information contained in this document will help you get the best functionality out of the Armadillo-9.

2. Precautions

2.1. Safety Precautions

Please read the following safety precautions carefully to assure correct use.



This product uses semiconductor components designed for generic electronics equipment such as office automation equipment, communications equipment, measurement equipment and machine tools. Do not incorporate the product into devices such as medical equipment, traffic control systems, combustion control systems, safety equipment and so on which can directly threaten human life or pose a hazard to the body or property due to malfunction or failure. Moreover, products incorporating semiconductor components can be caused to malfunction or fail due to foreign noise or surge. To ensure there will be no risk to life, the body or property even in the event of malfunction or failure, be sure to take all possible measures in the safety system design, such as using protection circuits like limit switches or fuse breakers, or system multiplexing.

2.2. Operational Precautions

To avoid a permanent damage to the Armadillo-9, the following precautions must be observed when handling the product.

- **Board Attachment/Detachment**
Do not attempt to attach or remove this board when power supply is being supplied to the Armadillo-9 or peripheral circuits.
- **Static Electricity**
The Armadillo-9 uses CMOS devices. Until the board is used, store it safely in the provided antistatic package.
- **Latch-up**
Due to excessive noise or surge from the power supply or input/output, sharp voltage fluctuations can lead to the CMOS devices incorporated in the board causing a latch-up. Once the latch-up occurs, this situation continues until the power supply is disconnected, and therefore can damage the devices. Measures such as adding a protection circuit to noise-susceptible input/output lines or not sharing the power supply with devices that can be cause of noise are highly recommended.

2.3. Software Precautions

- **Software contained in this product:**
The software and documentation contained in this product is provided "AS IS" without warranty of any kind including warranty of merchantability or fitness for a particular purpose, reliability, correctness or accuracy. Furthermore, we do not guarantee any outcomes resulting from the use of this product.

2.4. Trademarks

Armadillo is a registered trademark of Atmark Techno, Inc. Other products and company names are either trademarks or registered trademarks of their respective company or organization.

3. Overview

3.1. Board Overview

The main specifications of the Armadillo-9 are shown in Table 3-1.

Table 3-1 Armadillo-9 Board Specifications

| | |
|------------------------------|---|
| Processor | Cirrus Logic EP9315-CB Employs ARM920T core <ul style="list-style-type: none">• ARM9TDMI CPU• 16kByte Instruction Cache• 16kByte Data Cache• Thumb code (16bit instruction set) supported |
| System Clock | CPU Core Clock: 200MHz BUS Clock: 100MHz |
| Memory | SDRAM: 64MByte (32bit width) FLASH: 8MByte (16bit width) |
| LAN Interface | 10BASE-T/100BASE-TX |
| Serial Port | 2-CH (start/stop, Max: 115.2kbps) RS232C Level Input/Output Flow Control <ul style="list-style-type: none">• COM1: with flow control pins (CTS, RTS, DTR, DSR, DCD, RI)• COM2: no flow control pins |
| General Purpose Parallel I/O | 8 bits + 4 bits |
| Timer | <ul style="list-style-type: none">• 16-bit general purpose timer: 2 channels (one channel used for Linux system timer)• 32-bit general purpose timer: 1 channel• 40-bit debug timer: 1 channel |
| VGA | Connector Type: D-sub15 pin Max. Resolution: 1024×768 <ul style="list-style-type: none">• 1024×768 (8bit Color)• 800×600 (8/16bit Color)• 640×480 (8/16bit Color) |
| USB (Host) | 2.0 Full Speed (12Mbps) 1 channel, A-connector |
| Storage | IDE I/F (2.0mm-pitch, 44-pin) PIO Mode, ATA33 Mode support |
| Calendar Timer | SII: S-3531A (or S-35380A/S-35390A) Backup by polyacene capacitor (Off-board battery can be used in parallel) |
| Compact Flash | Type I/II (I/O, Memory Card) |
| Expansion Bus | PC/104-compliant pin assignment (16bit) |
| Board Size | 90.2 × 95.9 (not including protrusions) |
| Power Supply Voltage | 5V±5% |
| Consumption Current | 400mA (Typ.) |

3.2. Block Diagram

The block diagram of the Armadillo-9 is shown in Figure 3-1.

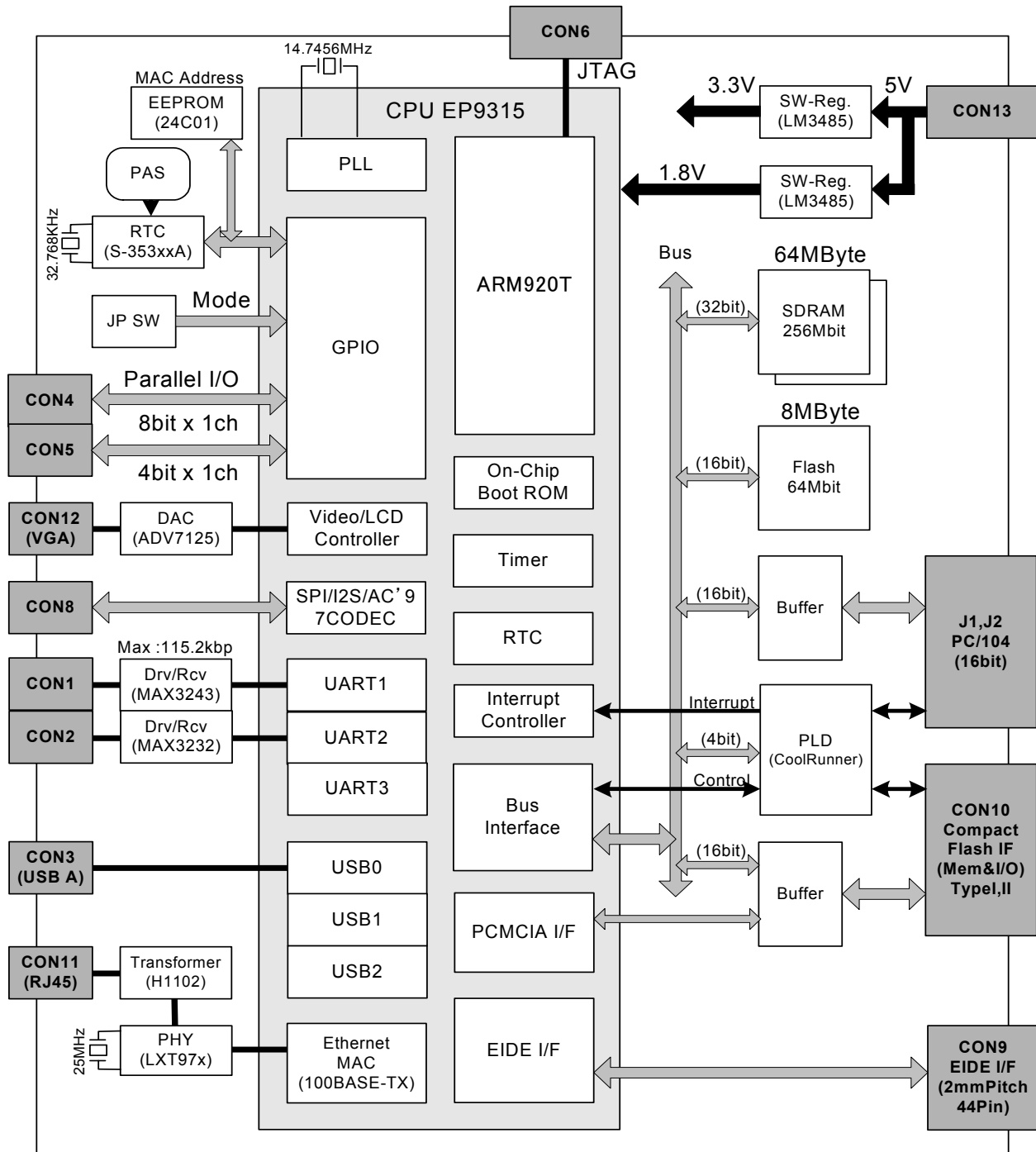


Figure 3-1 Block Diagram of Armadillo-9

4. Memory Map

4.1. Physical Memory Map

The physical memory map of the Armadillo-9 is shown in Table 4-1.

Table 4-1 Physical Memory Map of Armadillo-9

| Start Address | End Address | Device | Memory Area | Setting |
|---------------|-------------|---------------------------------|---------------------------|-------------|
| 0x0040 0000 | 0x0FFF FFFF | Reserved | CS0 | |
| 0x1000 0000 | 0x1000 000F | I/O Control Register | CS1 | 8bit width |
| 0x1000 0010 | 0x11FF FFFF | Reserved | | |
| 0x1200 0000 | 0x1200 FFFF | PC/104 I/O Space (8bit) | | |
| 0x1201 0000 | 0x12FF FFFF | Reserved | | |
| 0x1300 0000 | 0x13FF FFFF | PC/104 Memory Space (8bit) | | |
| 0x1400 0000 | 0x1FFF FFFF | Reserved | | |
| 0x2000 0000 | 0x21FF FFFF | Reserved | CS2 | 16bit width |
| 0x2200 0000 | 0x2200 FFFF | PC/104 I/O Space (16bit) | | |
| 0x2201 0000 | 0x22FF FFFF | Reserved | | |
| 0x2300 0000 | 0x23FF FFFF | PC/104 Memory Space (16bit) | | |
| 0x2400 0000 | 0x2FFF FFFF | Reserved | | |
| 0x3000 0000 | 0x3FFF FFFF | Reserved | | |
| 0x4000 0000 | 0x47FF FFFF | Compact Flash (I/O Space) | | 16bit width |
| 0x4800 0000 | 0x4BFF FFFF | Compact Flash (Attribute Space) | | 16bit width |
| 0x4C00 0000 | 0x4FFF FFFF | Compact Flash (Memory Space) | | 16bit width |
| 0x5000 0000 | 0x5FFFFFFF | Reserved | | |
| 0x6000 0000 | 0x607FFFFF | Flash Memory (8MByte) | CS6 | 16bit width |
| 0x60800000 | 0x6FFFFFFF | Reserved | | |
| 0x7000 0000 | 0x7FFF FFFF | Reserved | | |
| 0x8000 0000 | 0x8008 FFFF | EP9315 Internal Register (AHB) | CPU System Register | |
| 0x8009 0000 | 0x8009 3FFF | Internal Boot ROM (16KByte) | | |
| 0x8009 4000 | 0x8009 FFFF | Reserved | | |
| 0x800A 0000 | 0x800F FFFF | EP9315 Internal Register (AHB) | | |
| 0x8010 0000 | 0x807F FFFF | Reserved | | |
| 0x8080 0000 | 0x8094 FFFF | EP9315 Internal Register (APB) | | |
| 0x8095 0000 | 0x8FFF FFFF | Reserved | | |
| 0x9000 0000 | 0xBFFF FFFF | Reserved | | |
| 0xC000 0000 | 0xC1FF FFFF | SDRAM (32MByte) | SDCE0 (SDRAM) | 32bit width |
| 0xC200 0000 | 0xC3FF FFFF | Reserved | | |
| 0xC400 0000 | 0xC5FF FFFF | SDRAM (32MByte) | | |
| 0xC600 0000 | 0xCFFF FFFF | Reserved | | |
| 0xD000 0000 | 0xDFFF FFFF | Reserved | | |
| 0xE000 0000 | 0xEFFF FFFF | Reserved | | |
| 0xF000 0000 | 0xFFFF FFFF | Reserved | | |

4.2. Logical Memory Map When Using Linux

When Linux is being used, the Armadillo-9 is configured by the MMU with the following logical memory map.

Table 4-2 Armadillo-9 Logical Memory Map When Using Linux

| Start Address | End Address | Device | Memory Area | Setting |
|-----------------------|--------------|---------------------------------|---------------------------|-------------|
| Dynamically allocated | +0x0007 FFFF | Flash Memory (8MByte) | CS6 | 16bit width |
| 0xC000 0000 | 0xC3FF FFFF | SDRAM (64MByte) | SDCE0 (SDRAM) | 32bit width |
| 0xC400 0000 | 0xCFFF FFFF | Reserved | | |
| 0xD000 0000 | 0xD7FF FFFF | Compact Flash (I/O Space) | | 16bit width |
| 0xD800 0000 | 0xDBFF FFFF | Compact Flash (Attribute Space) | | 16bit width |
| 0xDC00 0000 | 0xDFFF FFFF | Compact Flash (Memory Space) | | 16bit width |
| 0xF000 0000 | 0xF000 000F | I/O Control Register | CS1 | 8bit width |
| 0xF000 0010 | 0xF1FF FFFF | Reserved | | |
| 0xF200 0000 | 0xF200 FFFF | PC/104 I/O Space (8bit) | | |
| 0xF201 0000 | 0xF2FF FFFF | Reserved | | |
| 0xF300 0000 | 0xF3FF FFFF | PC/104 Memory Space (8bit) | | |
| 0xF600 0000 | 0xF600 FFFF | PC/104 I/O Space (16bit) | CS2 | 16bit width |
| 0x F601 0000 | 0x F6FF FFFF | Reserved | | |
| 0x F700 0000 | 0x F7FF FFFF | PC/104 Memory Space (16bit) | | |
| 0xFF00 0000 | 0xFF08 FFFF | EP9315 Internal Register (AHB) | CPU System Register | |
| 0xFF09 0000 | 0xFF09 3FFF | Internal Boot ROM (16KByte) | | |
| 0xFF09 4000 | 0xFF09 FFFF | Reserved | | |
| 0xFF0A 0000 | 0xFF0F FFFF | EP9315 Internal Register (AHB) | | |
| 0xFF10 0000 | 0xFF7F FFFF | Reserved | | |
| 0xFF80 0000 | 0xFF94 FFFF | EP9315 Internal Register (APB) | | |
| 0xFF95 0000 | 0xFFFF FFFF | Reserved | | |

5. Interface Specifications

5.1. Interface Layout

The layout of the Armadillo-9's interfaces is shown in Figure 5-1.

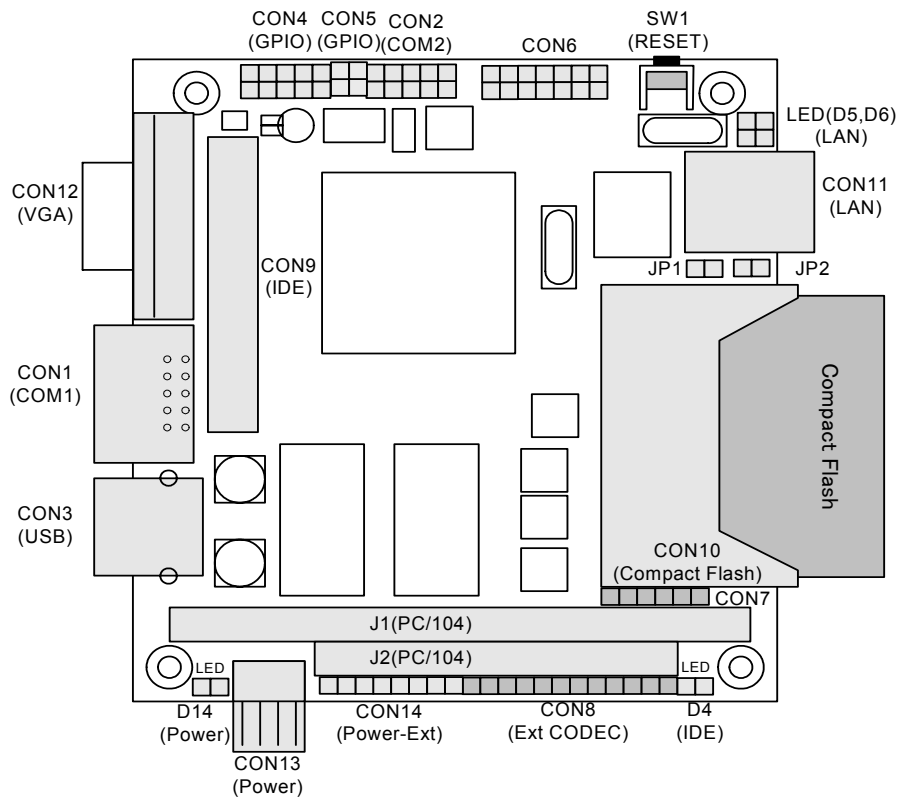


Figure 5-1 Interface Layout

Table 5-1 Interface Details

| Code | Interface | Remarks |
|-------------|---|------------------|
| CON1 | Serial Interface 1 | |
| CON2 | Serial Interface 2 | Not mounted |
| CON3 | USB Interface (Host, USB2.0, FullSpeed: 12Mbps) | Type-A connector |
| CON4 | Parallel Interface (8bit general purpose I/O) | Not mounted |
| CON5 | Parallel Interface (4bit general purpose I/O) | Not mounted |
| CON6 | JTAG Interface | Not mounted |
| CON7 | (Reserved) | Not mounted |
| CON8 | Synchronous Serial/AC97 CODEC/I2S CODEC | Not mounted |
| CON9 | IDE Interface (2.0mm pitch, 44-pin) | |
| CON10 | Compact Flash slot (Type I/II, I/O/Memory Card) | |
| CON11 | LAN Connector (10BASE-T/100BASE-TX) | RJ-45 |
| CON12 | VGA Interface (D-Sub15 pin) | |
| CON13 | Power Supply Input Terminal (5V, 12V) | |
| CON14 | Extension Power Supply Input Terminal (-5V, -12V, RTC backup) | No connector |
| J1, J2 | PC/104 Extension Connector (stack through) | No connector |
| LED (D4) | IDE Access | No connector |
| LED (D5, 6) | LAN Access ((Link, Active) | |
| LED (D14) | Power Supply | No connector |
| JP1, JP2 | Boot Mode Setting Jumpers | |
| SW1 | RESET Switch | |

5.2. CON1 (Serial Interface 1)

CON1 is an asynchronous (start-stop) serial interface. It is connected to UART1 on the CPU (EP9315).

- Signal input/output level: RS232C
- Maximum data rate: 115.2kbps
- Flow Control: CTS, RTS, DTR, DSR, DCD, RI
- FIFO: 16Byte built-in for both send and receive

Table 5-2 CON1 Signal Assignment

| No. | Signal Name | I/O | Function |
|-----|-------------|-------|--|
| 1 | DCD | I | Connects to EGPI01 (Port A: 1) pin of EP9315 |
| 2 | DSR | I | Connects to UART1-DSR pin of EP9315 |
| 3 | RXD | I | Connects to UART1-RXD pin of EP9315 |
| 4 | RTS | O | Connects to UART1-RTS pin of EP9315 |
| 5 | TXD | O | Connects to UART1-TXD pin of EP9315 |
| 6 | CTS | I | Connects to UART1-CTS pin of EP9315 |
| 7 | DTR | O | Connects to UART1-DTR pin of EP9315 |
| 8 | RI | I | Connects to EGPI00 (Port A: 0) pin of EP9315 |
| 9 | GND | Power | Power supply (GND) |
| 10 | +3.3V | Power | Power supply (+3.3V) |

5.3. CON2 (Serial Interface 2)

CON2 is an asynchronous (start-stop) serial interface. It is connected to UART2 on the CPU (EP9315).

- Signal input/output level: RS232C
- Maximum data rate: 115.2kbps
- Flow control: None
- FIFO: 16Byte built-in for both send and receive

Table 5-3 CON2 Signal Assignment

| No. | Signal Name | I/O | Function |
|-----|-------------|-------|--|
| 1 | - | | |
| 2 | - | | |
| 3 | RXD | I | Connects to UART2-RXD pin of EP9315 |
| 4 | RTS | O | Connects to CON2 (6-pin) on the board (loopback) |
| 5 | TXD | O | Connects to UART2-TXD pin of EP9315 |
| 6 | CTS | I | Connects to CON2 (4-pin) on the board (loopback) |
| 7 | - | | |
| 8 | - | | |
| 9 | GND | Power | Power supply (GND) |
| 10 | +3.3V | Power | Power supply (+3.3V) |

5.4. CON3 (USB Interface)

CON3 is a USB serial interface. It is connected to USB0 on the CPU (EP9315).

- Data Transfer Mode: USB2.0 Full Speed (12Mbps), Low Speed (1.5Mbps)
- Power Supply: Voltage: +5V, Current: 500mA(max)
- Connector Type: Type A

Table 5-4 CON3 Signal Assignment

| No. | Signal Name | I/O | Function |
|-----|-------------|-------|--------------------------------|
| 1 | +5V | Power | Power supply (+5V, max. 500mA) |
| 2 | USB- | I/O | Minus side USB signal |
| 3 | USB+ | I/O | Plus side USB signal |
| 4 | GND | Power | Power supply (GND) |

5.5. CON4 (Parallel Interface)

CON4 is a general purpose I/O port. It is connected to the GPIO (General Purpose I/O) on the CPU (EP9315). The port can be controlled using PADR (Port A data register I/O at 0x8084 0000), PADDDR (Port A data direction register I/O at 0x8084 0010), PBDR (Port B data register I/O at 0x8084 0004) and PBDDR (Port B data direction register I/O at 0x8084 0014) in the CPU.

Table 5-5 CON4 Signal Assignment

| No. | Signal Name | I/O | Function |
|-----|-------------|-------|---|
| 1 | GND | Power | Power supply (GND) |
| 2 | +3.3V | Power | Power supply (+3.3V) |
| 3 | GPIO_0 | I/O | GPIO port 0 (Connects to EGPIO4 (Port A: 4) pin of EP9315) |
| 4 | GPIO_1 | I/O | GPIO port 1 (Connects to EGPIO5 (Port A: 5) pin of EP9315) |
| 5 | GPIO_2 | I/O | GPIO port 2 (Connects to EGPIO6 (Port A: 6) pin of EP9315) |
| 6 | GPIO_3 | I/O | GPIO port 3 (Connects to EGPIO7 (Port A: 7) pin of EP9315) |
| 7 | GPIO_4 | I/O | GPIO port 4 (Connects to EGPIO8 (Port B: 0) pin of EP9315) |
| 8 | GPIO_5 | I/O | GPIO port 5 (Connects to EGPIO9 (Port B: 1) pin of EP9315) |
| 9 | GPIO_6 | I/O | GPIO port 6 (Connects to EGPIO10 (Port B: 2) pin of EP9315) |
| 10 | GPIO_7 | I/O | GPIO port 7 (Connects to EGPIO11 (Port B: 4) pin of EP9315) |

Electrical specifications of the parallel interface are shown in Table 5-6.

Table 5-6 Electrical Specifications of CON4 Parallel Interface

| Symbol | Parameter | Min | Max | Unit | Conditions |
|-----------------|--------------------------|------------------------|------------------------|------|---|
| V _{IH} | CMOS Input high voltage | 0.65×V _{DDIO} | V _{DDIO} +0.3 | V | V _{DDIO} =3.3V |
| V _{IL} | CMOS Input low voltage | -0.3 | 0.35×V _{DDIO} | V | |
| V _{OH} | CMOS Output high voltage | 2.8 | | V | I _{OH} =4mA |
| V _{OL} | CMOS Output low voltage | | 0.5 | V | I _{OL} =-4mA |
| I _{OH} | CMOS Output high voltage | | 4 | mA | |
| I _{OL} | CMOS Output low voltage | | -4 | mA | |
| I _{IL} | Input leakage current | | 10.0 | μA | V _{IN} =V _{DD} or GND |

5.6. CON5 (Parallel Interface)

CON5 is a general purpose I/O port. It is connected to the GPIO (General Purpose I/O) of the CPU (EP9315). The port can be controlled using PDDR (Port D data register I/O at 0x8084 000C) and PDDDR (Port D data direction register I/O at 0x8084 001C) in the CPU. The electrical specifications of the CON5 parallel interface are as shown in Table 5-6.

Table 5-7 CON5 Signal Assignment

| No. | Signal Name | I/O | Function |
|-----|-------------|-----|---|
| 1 | GPIO_Ext0 | I/O | GPIO port 0 (Connects to Port D: 4 pin of EP9315) |
| 2 | GPIO_Ext1 | I/O | GPIO port 1 (Connects to Port D: 5 pin of EP9315) |
| 3 | GPIO_Ext2 | I/O | GPIO port 2 (Connects to Port D: 6 pin of EP9315) |
| 4 | GPIO_Ext3 | I/O | GPIO port 3 (Connects to Port D: 7 pin of EP9315) |

5.7. CON6 (EP9315 JTAG)

The CON6 connector is used to connect a JTAG debugger to the Armadillo-9. It is connected to the JTAG signal on the CPU (EP9315).

| No. | Signal Name | I/O | Function |
|-----|-------------|-------|----------------------|
| 1 | +3.3V | Power | Power supply (+3.3V) |
| 2 | GND | Power | Power supply (GND) |
| 3 | TRST* | I | JTAG TRST* on EP9315 |
| 4 | GND | Power | Power supply (GND) |
| 5 | TDI | I | JTAG TDI on EP9315 |
| 6 | GND | Power | Power supply (GND) |
| 7 | TMS | I | JTAG TMS on EP9315 |
| 8 | GND | Power | Power supply (GND) |
| 9 | TCK | I | JTAG TCK on EP9315 |
| 10 | GND | Power | Power supply (GND) |
| 11 | TDO | O | JTAG TDO on EP9315 |
| 12 | - | | (Reserved) |
| 13 | +3.3V | Power | Power supply (+3.3V) |
| 14 | GND | Power | Power supply (GND) |

5.8. CON7

Normal operation is not guaranteed when using this connector.

5.9. CON8 (Synchronous Serial / AC97 / I2S)

While the CON8 connector is used to connect a synchronous serial, AC97CODEC or audio CODEC device, normal operation of the Armadillo9 is not guaranteed when using this connector. Table 5-8 shows the pin assignment.

Table 5-8 CON8 Signal Assignment

| No. | Signal Name | I/O | Function |
|-----|-------------|-------|----------------------------------|
| 1 | GND | Power | Power supply (GND) |
| 2 | ASDI | I | Refer to Table 5-9 (PU: ASDI) |
| 3 | ARST* | O | Refer to Table 5-9 (CPU: ARST*) |
| 4 | ASDO | O | Refer to Table 5-9 CPU: ASDO) |
| 5 | ASYNC | | Refer to Table 5-9 (CPU: ASYNC) |
| 6 | ABITCLK | | Refer to Table 5-9 CPU: BITCLK) |
| 7 | +3.3V | Power | Power supply (+3.3V) |
| 8 | SSPRX1 | I | Refer to Table 5-9 (CPU: SSPRX1) |
| 9 | SSPTX1 | O | Refer to Table 5-9 (CPU: SSPTX1) |
| 10 | FREM1 | | Refer to Table 5-9 (CPU: SFRM1) |
| 11 | SCLK1 | | Refer to Table 5-9 (CPU: SCLK1) |
| 12 | GND | Power | Power supply (GND) |

The functionality assigned to the CON8 pins can be switched by setting the EP9315 register. Three modes are available: "Normal Mode", "I2S on AC97 Mode" and "I2S on SSP Mode", which can be selected by rewriting "bit6: I2S on AC97" and "bit7: I2S on SSP" of the DeviceCfg Register at 0x8093 0080.

Table 5-9 Pin Functionality in Each Mode

| Pin Name | Normal Mode | I2S on AC97 Mode | I2S on SSP Mode |
|----------|--------------------|--------------------|-------------------|
| SSPRX1 | SPI Serial Input | I2S Serial Input | SPI Serial Input |
| SSPTX1 | SPI Serial Output | I2S Serial Output | SPI Serial Output |
| SFRM1 | SPI Frame Clock | I2S Frame Clock | SPI Frame Clock |
| SCLK1 | SPI Bit Clock | I2S Serial Clock | SPI Bit Clock |
| ASDI | AC97 Serial Input | AC97 Serial Input | I2S Serial Input |
| ASDO | AC97 Serial Output | AC97 Serial Output | I2S Serial Output |
| ASYNC | AC97 Frame Clock | AC97 Frame Clock | I2S Frame Clock |
| ABITCLK | AC97 Bit Clock | AC97 Bit Clock | I2S Serial Clock |
| ARST* | AC97 Reset | AC97 Reset | I2S Master Clock |

5.10. CON9 (IDE Interface)

CON9 is a 2-mm, 44-pin connector used to connect an IDE device. A 2.5-inch hard-disk drive can be connected using a straight flat cable. PIO mode and ATA33 data transfer modes are supported. The following table shows the pin assignment of CON9.

Table 5-10 CON9 Signal Assignment

| No. | Signal Name | I/O | Function |
|-----|-------------|-------|--------------------|
| 1 | RESET* | O | Reset signal |
| 2 | GND | Power | Power supply (GND) |
| 3 | DD7 | I/O | Data bus (bit7) |
| 4 | DD8 | I/O | Data bus (bit8) |
| 5 | DD6 | I/O | Data bus (bit6) |
| 6 | DD9 | I/O | Data bus (bit9) |
| 7 | DD5 | I/O | Data bus (bit5) |
| 8 | DD10 | I/O | Data bus (bit10) |
| 9 | DD4 | I/O | Data bus (bit4) |
| 10 | DD11 | I/O | Data bus (bit11) |
| 11 | DD3 | I/O | Data bus (bit3) |
| 12 | DD12 | I/O | Data bus (bit12) |
| 13 | DD2 | I/O | Data bus (bit2) |
| 14 | DD13 | I/O | Data bus (bit13) |
| 15 | DD1 | I/O | Data bus (bit1) |
| 16 | DD14 | I/O | Data bus (bit14) |
| 17 | DD0 | I/O | Data bus (bit0) |
| 18 | DD15 | I/O | Data bus (bit15) |
| 19 | GND | Power | Power supply (GND) |
| 20 | NC | - | Not supported |
| 21 | DMARQ | I | DMA request |
| 22 | GND | Power | Power supply (GND) |
| 23 | DIOW* | O | I/O write enable |
| 24 | GND | Power | Power supply (GND) |
| 25 | DIOR* | O | I/O read enable |
| 26 | GND | Power | Power supply (GND) |
| 27 | IORDY | I | IO ready |
| 28 | CSEL | O | Cable select (GND) |
| 29 | DMACK* | O | DMA acknowledge |
| 30 | GND | Power | Power supply (GND) |
| 31 | INTRQ | I | Interrupt request |
| 32 | NC | - | Not supported |
| 33 | DA1 | O | Address bus (bit1) |
| 34 | NC | - | Not supported |
| 35 | DA0 | O | Address bus (bit0) |
| 36 | DA2 | O | Address bus (bit2) |
| 37 | CS0* | O | Chip select 0 |
| 38 | CS1* | O | Chip select 1 |
| 39 | DASP* | I | Device access |
| 40 | GND | Power | Power supply (GND) |
| 41 | +5V | Power | Power supply (+5V) |
| 42 | +5V | Power | Power supply (+5V) |
| 43 | GND | Power | Power supply (GND) |
| 44 | NC | - | Not supported |

5.11. CON10 (Compact Flash)

CON10 is a Compact Flash interface. It supports I/O mode and memory mode, allowing the connection of ATA devices and I/O cards.

- Connection Modes: I/O Mode, Memory Mode
- Type: Type I, Type II
- 3.3V cards only, Hot Plug support

Table 5-11 CON10 Signal Assignment

| No. | Signal Name | I/O | Function |
|-----|-------------|-------|-----------------------------|
| 1 | GND | Power | Power supply (GND) |
| 2 | D3 | I/O | Data bus (bit3) |
| 3 | D4 | I/O | Data bus (bit4) |
| 4 | D5 | I/O | Data bus (bit5) |
| 5 | D6 | I/O | Data bus (bit6) |
| 6 | D7 | I/O | Data bus (bit7) |
| 7 | CE1* | O | Card enable signal 1 |
| 8 | A10 | O | Address bus (bit10) |
| 9 | OE* | O | Data out enable |
| 10 | A9 | O | Address bus (bit9) |
| 11 | A8 | O | Address bus (bit8) |
| 12 | A7 | O | Address bus (bit7) |
| 13 | +3.3V | Power | Power supply (+3.3V) |
| 14 | A6 | O | Address bus (bit6) |
| 15 | A5 | O | Address bus (bit5) |
| 16 | A4 | O | Address bus (bit4) |
| 17 | A3 | O | Address bus (bit3) |
| 18 | A2 | O | Address bus (bit2) |
| 19 | A1 | O | Address bus (bit1) |
| 20 | A0 | O | Address bus (bit0) |
| 21 | D0 | I/O | Data bus (bit0) |
| 22 | D1 | I/O | Data bus (bit1) |
| 23 | D2 | I/O | Data bus (bit2) |
| 24 | IOCS16* | I | I/O 16bit |
| 25 | CD2* | I | Card detection |
| 26 | CD1* | I | Card detection |
| 27 | D11 | I/O | Data bus (bit11) |
| 28 | D12 | I/O | Data bus (bit12) |
| 29 | D13 | I/O | Data bus (bit13) |
| 30 | D14 | I/O | Data bus (bit14) |
| 31 | D15 | I/O | Data bus (bit15) |
| 32 | CE2* | O | Card enable signal 2 |
| 33 | VS1* | | |
| 34 | IORD* | O | I/O read enable |
| 35 | IOWR* | O | I/O write enable |
| 36 | WE* | O | Write enable |
| 37 | IREQ | I | Interrupt request |
| 38 | +3.3V | Power | Power supply (+3.3V) |
| 39 | NC | - | - |
| 40 | VS2* | | |
| 41 | RESET* | O | Reset |
| 42 | WAIT* | I | Ready |
| 43 | - | - | |
| 44 | REG* | O | Register select, I/O enable |
| 45 | BVD2 | I | |
| 46 | BVD1 | I | |
| 47 | D8 | I/O | Data bus (bit8) |
| 48 | D9 | I/O | Data bus (bit9) |
| 49 | D10 | I/O | Data bus (bit10) |
| 50 | GND | Power | Power supply (GND) |

5.12. CON11 (LAN Connector)

CON11 is a 10BASE-T/100BASE-TX LAN interface used to connect a category 5 or higher Ethernet cable. While it is normally used to connect to a hub using a straight cable, it can also be used to directly connect a PC etc. using a cross-cable.

Table 5-12 CON11 Signal Assignment

| No. | Signal Name | I/O | Function |
|-----|-------------|-----|---|
| 1 | TX+ | O | Differential twist pair transmit output (+) |
| 2 | TX- | O | Differential twist pair transmit output (-) |
| 3 | RX+ | I | Differential twist pair receive input (+) |
| 4 | - | - | |
| 5 | - | - | |
| 6 | RX- | I | Differential twist pair receive input (-) |
| 7 | - | - | |
| 8 | - | - | |

5.13. CON12 (VGA Connector)

CON12 is a VGA connector (D-SUB15 pin) used to connect a standard CRT or LCD display.

Table 5-13 CON12 Signal Assignment

| No. | Signal Name | I/O | Function |
|-----|-------------|-------|-------------------------------|
| 1 | RED | O | Analog, color signal (red) |
| 2 | GREEN | O | Analog, color signal (green) |
| 3 | BLUE | O | Analog, color signal (blue) |
| 4 | - | - | - |
| 5 | GND | Power | Signal ground (GND) |
| 6 | GND | Power | Signal ground (GND) |
| 7 | GND | Power | Signal ground (GND) |
| 8 | GND | Power | Signal ground (GND) |
| 9 | - | - | - |
| 10 | GND | Power | Signal ground (GND) |
| 11 | - | - | - |
| 12 | - | - | - |
| 13 | H_SYNC | O | Horizontal synchronous signal |
| 14 | V_SYNC | O | Vertical synchronous signal |
| 15 | - | - | - |

Table 5-14 Resolution and Horizontal Frequency

| Resolution | Colors | Horizontal Frequency (Vertical Frequency) |
|------------|---------|---|
| 640×480 | 8/16bit | 31.5kHz (60Hz) |
| 800×600 | 8/16bit | 37.9kHz (60Hz) |
| 1024×768 | 8bit | 48.4kHz (60Hz) |

5.14. CON13 (Power Input Connector)

The CON13 connector used is to connect a power supply to the Armadillo-9. The minimum power supply required to operate the Armadillo-9 is +5V-GND. The +12V is connected to the PC/104 +12V supply pin.

Table 5-15 CON13 Signal Assignment

| No. | Signal Name | I/O | Function |
|-----|-------------|-------|---|
| 1 | +5V | Power | Power input (+5V) Supplies to the PC/104 +5V pin and the IDE +5V pin |
| 2 | GND | Power | Power supply (GND) |
| 3 | GND | Power | Power supply (GND) |
| 4 | +12V | Power | Power input (+12V) * Supplies to the PC/104 +12V pin |

* Not specifically required for the operation of the Armadillo-9.

5.15. CON14 (Extension Power Input)

CON14 is a power supply connector for the Armadillo-9.

Table 5-16 CON14 Signal Assignment

| No. | Signal Name | I/O | Function |
|-----|-------------|-------|--|
| 1 | GND | Power | Power supply (GND) |
| 2 | BAT | Power | Power input for backup of RTC (S-353xxA) * |
| 3 | GND | Power | Power supply (GND) |
| 4 | EXTIRQ* | I/O | Connectable to the EXTIRQ* input of the CPU (EP9315) by shorting JP3. Connectable to the INT output of the RTC(S-353xxA) by shorting JP4. |
| 5 | GND | Power | Power supply (GND) |
| 6 | -5V | Power | Power input (-5V) * Supplies to the PC/104 -5V pin |
| 7 | GND | Power | Power supply (GND) |
| 8 | -12V | Power | Power input (-12V) * Supplies to the PC/104 -12V pin |

* Not specifically required for the operation of the Armadillo-9.

5.16. J1, J2 (PC/104-Compliant Extension Bus)

J1 and J2 are extension buses with PC/104-compliant bus arrays. They have a 64kB I/O area and a 16MB memory area. However, since the ARM architecture does not have an I/O area (I/O access only) as x86 CPUs do, the I/O area is placed in the standard memory space.

The extension buses are a subset of the PC/104 standard. Main differences with the standard PC/104 bus are as follows:

- Non-support of dynamic bus sizing
- Non-support of DMA (DREQ / DACK)
- Non-support of external master
- Fixed bus access cycle

Table 5-17 J1 Signal Assignment (1)

| No. | Signal Name | I/O | Function |
|-----|-------------|-------|---|
| A1 | IOCHCHK* | (I) | Non-support |
| A2 | D7 | I/O | Data bus (bit7) |
| A3 | D6 | I/O | Data bus (bit6) |
| A4 | D5 | I/O | Data bus (bit5) |
| A5 | D4 | I/O | Data bus (bit4) |
| A6 | D3 | I/O | Data bus (bit3) |
| A7 | D2 | I/O | Data bus (bit2) |
| A8 | D1 | I/O | Data bus (bit1) |
| A9 | D0 | I/O | Data bus (bit0) |
| A10 | IOCHRDY* | I | Extension of access cycle to match a low speed device |
| A11 | AEN | O | Release of bus (GND) |
| A12 | A19 | O | Address bus (bit19) |
| A13 | A18 | O | Address bus (bit18) |
| A14 | A17 | O | Address bus (bit17) |
| A15 | A16 | O | Address bus (bit16) |
| A16 | A15 | O | Address bus (bit15) |
| A17 | A14 | O | Address bus (bit14) |
| A18 | A13 | O | Address bus (bit13) |
| A19 | A12 | O | Address bus (bit12) |
| A20 | A11 | O | Address bus (bit11) |
| A21 | A10 | O | Address bus (bit10) |
| A22 | A9 | O | Address bus (bit9) |
| A23 | A8 | O | Address bus (bit8) |
| A24 | A7 | O | Address bus (bit7) |
| A25 | A6 | O | Address bus (bit6) |
| A26 | A5 | O | Address bus (bit5) |
| A27 | A4 | O | Address bus (bit4) |
| A28 | A3 | O | Address bus (bit3) |
| A29 | A2 | O | Address bus (bit2) |
| A30 | A1 | O | Address bus (bit1) |
| A31 | A0 | O | Address bus (bit0) |
| A32 | GND | Power | Power supply (GND) |

Table 5-18 J1 Signal Assignment (2)

| No. | Signal Name | I/O | Function |
|-----|-------------|-------|----------------------------------|
| B1 | GND | Power | Power supply (GND) |
| B2 | RESET_DRV | O | Reset output |
| B3 | +5V | Power | Power supply (+5V) |
| B4 | IRQ9 | I | Interrupt 9 |
| B5 | -5V | Power | Power supply (-5V) |
| B6 | DQR2 | (I) | Non-support |
| B7 | -12V | Power | Power supply (-5V) |
| B8 | ENDXFR* | (I) | Non-support (5V pull-up) |
| B9 | +12V | Power | Power supply (+12V) |
| B10 | (KEY) | - | GND |
| B11 | SMEMW* | O | Memory write strobe |
| B12 | SMEMR* | O | Memory read strobe |
| B13 | IOW* | O | I/O write strobe |
| B14 | IOR* | O | I/O read strobe |
| B15 | DACK3* | (O) | Non-support (3.3V pull-up) |
| B16 | DRQ3 | (I) | Non-support |
| B17 | DACK1* | (O) | Non-support (3.3V pull-up) |
| B18 | DRQ1 | (I) | Non-support |
| B19 | REFRESH* | (O) | Non-support (3.3V pull-up) |
| B20 | SYSCLK | O | 8.333MHz (1/12 of CPU bus clock) |
| B21 | IRQ7 | I | Interrupt request 7 |
| B22 | IRQ6 | I | Interrupt request 6 |
| B23 | IRQ5 | I | Interrupt request 5 |
| B24 | IRQ4 | I | Interrupt request 4 |
| B25 | IRQ3 | I | Interrupt request 3 |
| B26 | DACK2* | (O) | Non-support (3.3V pull-up) |
| B27 | T/C | (O) | Non-support (3.3V pull-up) |
| B28 | BALE | O | Address latch enable |
| B29 | +5V | Power | Power supply (+5V) |
| B30 | OSC | (O) | Non-support (OPEN) |
| B31 | GND | Power | Power supply (GND) |
| B32 | GND | Power | Power supply (GND) |

Table 5-19 J2 Signal Assignment (1)

| No. | Signal Name | I/O | Function |
|-----|-------------|-------|--|
| C0 | GND | Power | Power supply (GND) |
| C1 | SBHE* | O | Bus high enable (active when the high 8-bit on data bus is used) |
| C2 | A23 | O | Address bus (23bit) |
| C3 | A22 | O | Address bus (22bit) |
| C4 | A21 | O | Address bus (21bit) |
| C5 | A20 | O | Address bus (20bit) |
| C6 | A19 | O | Address bus (19bit) |
| C7 | A18 | O | Address bus (18bit) |
| C8 | A17 | O | Address bus (17bit) |
| C9 | MEMR* | O | Memory read strobe |
| C10 | MEMW* | O | Memory write strobe |
| C11 | D8 | I/O | Data bus (bit8) |
| C12 | D9 | I/O | Data bus (bit9) |
| C13 | D10 | I/O | Data bus (bit10) |
| C14 | D11 | I/O | Data bus (bit11) |
| C15 | D12 | I/O | Data bus (bit12) |
| C16 | D13 | I/O | Data bus (bit13) |
| C17 | D14 | I/O | Data bus (bit14) |
| C18 | D15 | I/O | Data bus (bit15) |
| C19 | (KEY) | - | GND |

Table 5-20 J2 Signal Assignment (2)

| No. | Signal Name | I/O | Function |
|-----|-------------|-------|----------------------------|
| D0 | GND | Power | Power supply (GND) |
| D1 | MEMCS16* | (I) | Non-support (5V pull-up) |
| D2 | IOCS16* | (I) | Non-support (5V pull-up) |
| D3 | IRQ10 | I | Interrupt request 10 |
| D4 | IRQ11 | I | Interrupt request 11 |
| D5 | IRQ12 | I | Interrupt request 12 |
| D6 | IRQ15 | I | Interrupt request 15 |
| D7 | IRQ14 | I | Interrupt request 14 |
| D8 | DACK0* | (O) | Non-support (3.3V pull-up) |
| D9 | DREQ0 | (I) | Non-support |
| D10 | DACK5* | (O) | Non-support (3.3V pull-up) |
| D11 | DREQ5 | (I) | Non-support |
| D12 | DACK6* | (O) | Non-support (3.3V pull-up) |
| D13 | DREQ6 | (I) | Non-support |
| D14 | DACK7* | (O) | Non-support (3.3V pull-up) |
| D15 | DREQ7 | (I) | Non-support |
| D16 | +5V | Power | Power supply (+5V) |
| D17 | MASTER* | (I) | Non-support (5V pull-up) |
| D18 | GND | Power | Power supply (GND) |
| D19 | GND | Power | Power supply (GND) |

5.16.1. Precautions for PC/104 Extension Bus Access

As the PC/104 extension bus of the Armadillo-9 is not equipped with a dynamic bus sizing function, care is needed when accessing the PC/104 I/O area or memory area.

The Armadillo-9 has one physical I/O area (64kB) and one physical memory area (16MB). These two physical areas can each be accessed from two virtual areas (8bit and 16bit). Using either virtual area accesses the same physical area.

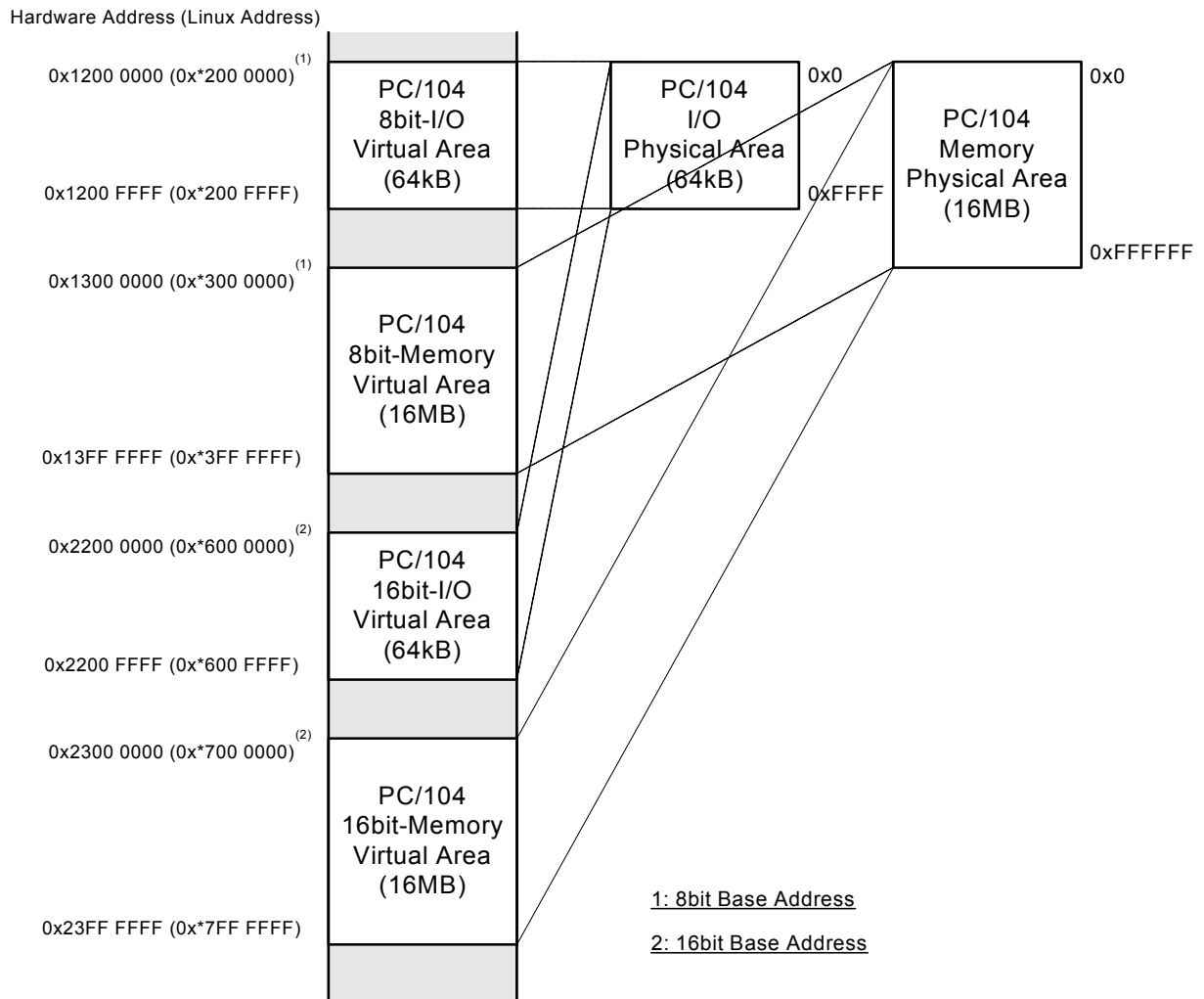


Figure 5-2 Memory Space of PC/104 Bus

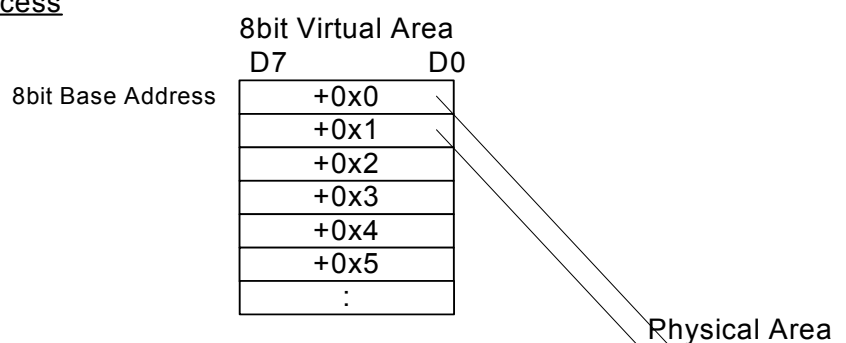
Each virtual area can be used as follows.

| | |
|--------------------|---|
| 8bit virtual area | • 8-bit access using data bus (D7 - D0) |
| 16bit virtual area | • 8-bit access to odd numbered addresses using data bus (D15 - D8) • 8-bit access to even numbered addresses using data bus (D7 - D0) • 16-bit access using data bus (D15 - D0) |

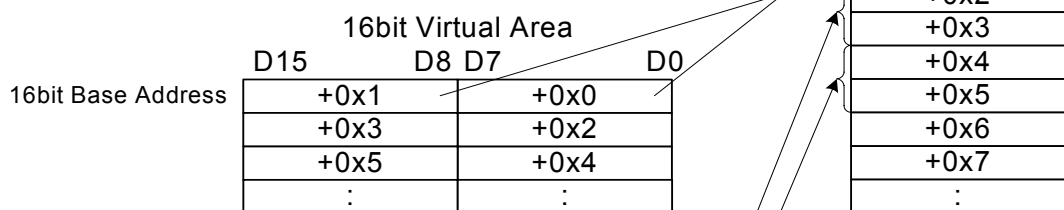
Accessing the physical areas can be accomplished as follows:

8(16)bit Base Address + Physical Area offset Address

8bit Physical Area Access



16bit Physical Area 8bit Access



16bit Physical Area 16bit Access

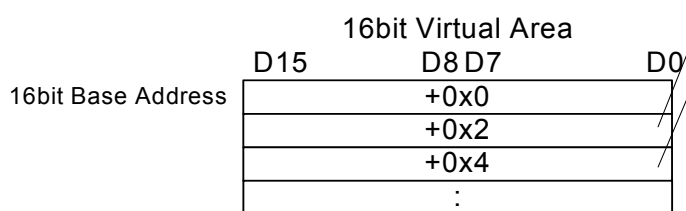


Figure 5-3 Method to Access PC/104 Bus

5.16.2. Access Timing

The figure below shows the access timing to the PC/104 extension bus. The access timing is the same for both 16bit and 8bit access.

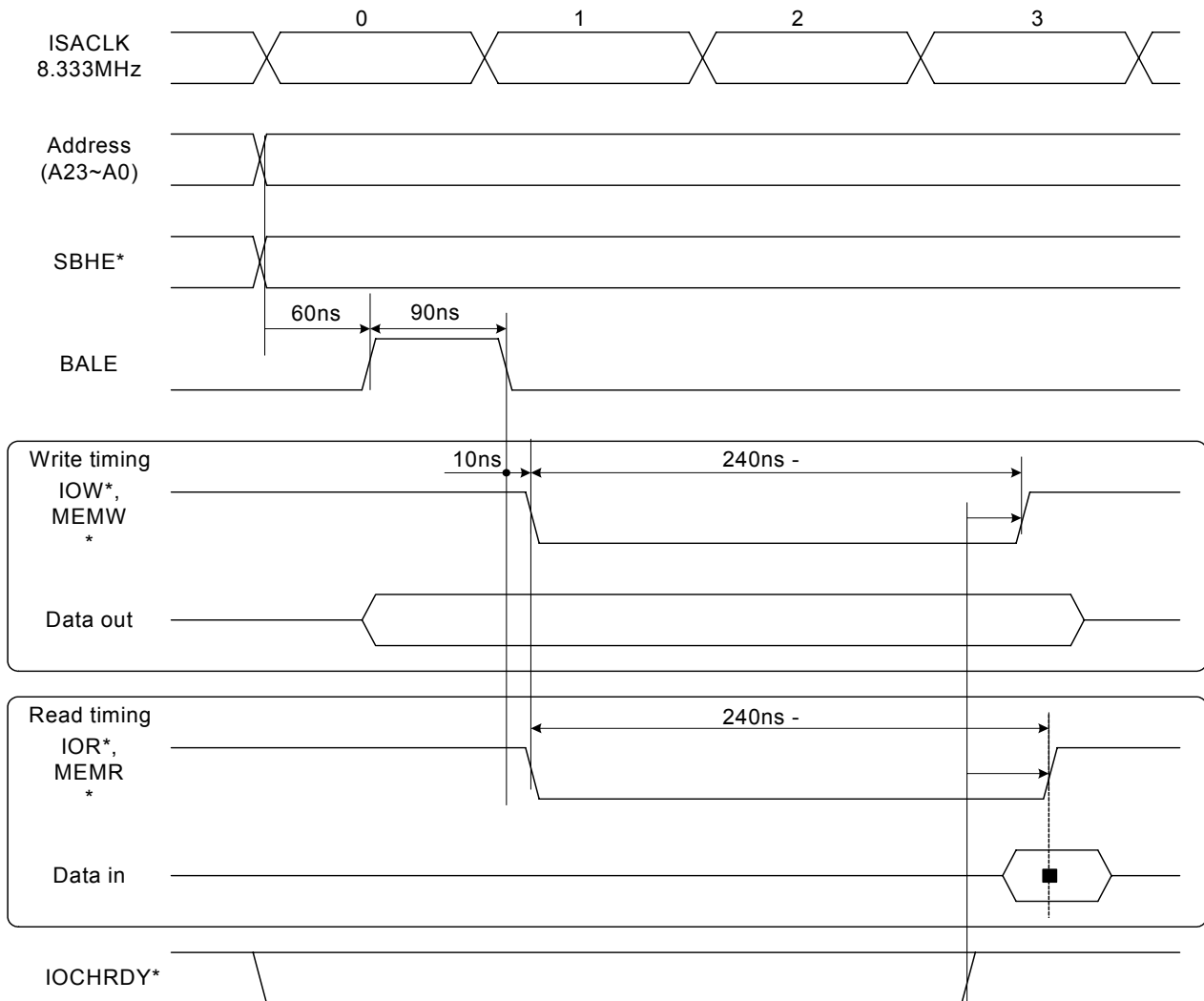


Figure 5-4 PC/104 Bus Access Timing

5.17. LED (D4)

LED (D4) is the IDE access lamp.

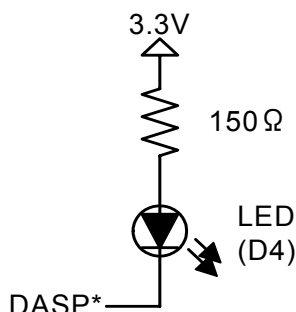


Figure 5-5 LED (D4) Connections

5.18. LED (D5, D6)

LED (D5,6) show the LAN status.

Table 5-21 Status of LED (D5, D6)

| Code | Name | ON | OFF |
|------|------|--|--|
| D5 | LINK | A LAN cable is connected and a 10BASE-T or 100BASE-TX link is established. | A LAN cable is not connected or connecting device is not in active mode. |
| D6 | LAN | Data is being transmitted/received. | No data is being transmitted/received. |

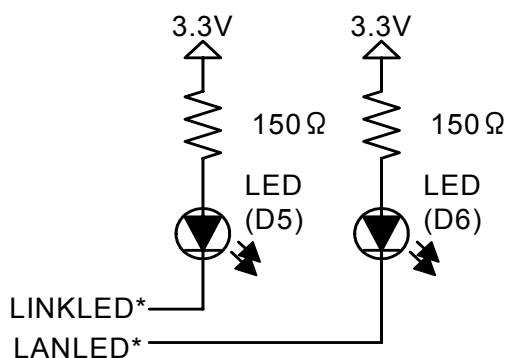


Figure 5-6 LED (D5, 6) Connections

5.19. LED (D14)

The LED (D14) indicates the status of the Armadillo-9's power supply.

Table 5-22 Status of LED (D14)

| Code | Name | ON | OFF |
|------|-------|---|---|
| D14 | POWER | The Armadillo-9 is being supplied power | The Armadillo-9 is not being supplied power |

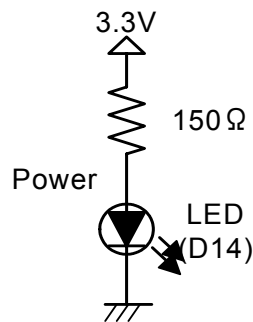


Figure 5-7 LED(D14) Connections

5.20. JP1-2

JP1, 2 are used to set the boot mode of the Armadillo-9.

5.20.1. JP1 (Boot ROM Selection)

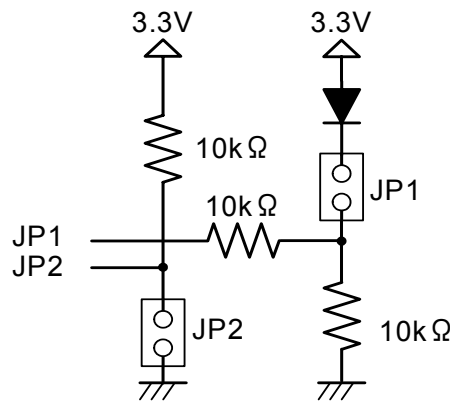
Either on-board Flash memory or on-chip boot ROM can be selected as the boot device. The on-chip boot ROM is used when executing a program downloaded via the serial (COM1) and rewriting the on-board Flash memory. For more information on the on-chip boot ROM, refer to "EP9315 User's Guide".

5.20.2. JP2 (Boot Linux Selection)

JP2 allows selection of the device storing the Linux Kernel. This JP setting is effective only when Linux is installed.

Table 5-23 Jumper Settings and Function

| JP1 | JP2 | Boot Device | Boot Kernel |
|-----|-----|-----------------------|---|
| OFF | OFF | On-board Flash memory | Linux Kernel of on-board Flash memory |
| OFF | ON | On-board Flash memory | (1) If an IDE device is installed: Linux Kernel of IDE device is booted. (2) If Compact Flash is installed: Linux Kernel of Compact Flash is booted. (3) Neither an IDE device or CompactFlash is installed: Boot loader "Hermit" is booted. (4) A Linux Kernel is not found in either the IDE device or CompactFlash: Boot loader "Hermit" is booted. |
| ON | - | On-chip boot ROM | On-chip boot ROM program is booted. |


Figure 5-8 Jumper Connector

5.21. Connector Type

Table 5-24 shows connector types of CON1-14 and J1-2.

Table 5-24 List of Connector Types

| Connector | Vendor | Type | Remarks |
|-----------|-----------------|----------------------|--|
| CON1 | Hirose Electric | HIF3F-10PA-2.54DS | |
| CON2 | - | 2×5 (2.54mm pitch) | (not mounted) |
| CON3 | JST Mfg. | UBA-4 R-S10-2 | Surface mount |
| CON4 | - | 2×5 (2.54mm pitch) | (not mounted) |
| CON5 | - | 2×2 (2.54mm pitch) | (not mounted) |
| CON6 | - | 2×7 (2.54mm pitch) | (not mounted) |
| CON7 | - | 1×6 (2.54mm pitch) | (not mounted) |
| CON8 | - | 1×12 (2.54mm pitch) | (not mounted) |
| CON9 | Hirose Electric | A3A-44PA-2SV | IDE (2.0mm pitch, 44-pin) |
| CON10 | DDK | MCD-CEN750PC | Compact Flash (Type I, II) |
| CON11 | FRE | E5388-F00214 | RJ-45 connector |
| CON12 | JST Mfg. | KSEY-15S-3B6L19-13 | VGA surface mount connector |
| CON13 | AMP | 171826-4 | Power connector |
| CON14 | - | 1×8 (2.54mm pitch) | (not mounted) |
| J1 | Astron | AT-ES1-64-12-2GF | PC/104 J1 stack through (not mounted) |
| J2 | Astron | AT-ES1-20-12-1GF (2) | PC/104 J2 stack through (not mounted) |

5.22. LED Types (Reference)

Examples of the LED types that can be connected to the Armadillo-9 are shown in Table 5-25.

| Connector | Vendor | Type | Color |
|-----------|----------|--------------------------|-------------|
| D4 | Toshiba | TLR123 and similar | Red |
| D1, 2 | Dialight | 553-0112-200 and similar | Red / Green |
| D14 | Toshiba | TLG123A and similar | Green |

Table 5-25 LED Types

6. Other Functions

6.1. CPLD Internal Register (I/O Control Register)

6.1.1. Memory Map of I/O Control Register

The Armadillo-9 CPLD provides an I/O control register to control the PC/104 I/O. The memory map of the I/O control register is shown in Table 6-1.

Table 6-1 Memory Map of I/O Control Register

| Hardware Address | Linux Address | Read | Write |
|------------------|---------------|-----------------------------|---------------------------|
| 0x1000 0000 | 0xF000 0000 | Interrupt Service Register0 | Interrupt Clear Register0 |
| 0x1000 0001 | 0xF000 0001 | (Reserved) | (Reserved) |
| 0x1000 0002 | 0xF000 0002 | Interrupt Service Register1 | Interrupt Clear Register1 |
| 0x1000 0003 | 0xF000 0003 | (Reserved) | (Reserved) |
| 0x1000 0004 | 0xF000 0004 | Interrupt Service Register2 | Interrupt Clear Register2 |
| 0x1000 0005 | 0xF000 0005 | (Reserved) | (Reserved) |
| 0x1000 0006 | 0xF000 0006 | (Reserved) | (Reserved) |
| 0x1000 0007 | 0xF000 0007 | (Reserved) | (Reserved) |
| 0x1000 0008 | 0xF000 0008 | (Reserved) | Interrupt Mask Register0 |
| 0x1000 0009 | 0xF000 0009 | (Reserved) | (Reserved) |
| 0x1000 000A | 0xF000 000A | (Reserved) | Interrupt Mask Register1 |
| 0x1000 000B | 0xF000 000B | (Reserved) | (Reserved) |
| 0x1000 000C | 0xF000 000C | (Reserved) | Interrupt Mask Register2 |
| 0x1000 000D | 0xF000 000D | (Reserved) | (Reserved) |
| 0x1000 000E | 0xF000 000E | (Reserved) | ISA mode Control Register |
| 0x1000 000F | 0xF000 000F | (Reserved) | (Reserved) |

- **Interrupt Service Register:**
A register to read the received interrupt factor.
- **Interrupt Clear Register**
A register to clear the interrupt factor received in the interrupt service register.
- **Interrupt Mask Register**
A register to mask the input of various interrupts.
- **ISA mode Control Register**
A register to set the PC/104 (ISA) transfer mode.

6.1.2. Details of the I/O Control Registers

Table 6-2 gives details of the I/O Control registers.

Table 6-2 Details of I/O Control Registers

| Register name | Hardware Address | Linux Address | Data | | | | | | | |
|-----------------------------|------------------|---------------|------|---|---|---|-------|-----------|----------|-------|
| | | | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Read Only | | | | | | | | | | |
| Interrupt Service Register0 | 0x1000 0000 | 0xF000 0000 | - | - | - | - | - | IRQ15 | IRQ14 | IRQ12 |
| Interrupt Service Register1 | 0x1000 0002 | 0xF000 0002 | - | - | - | - | IRQ11 | IRQ10 | IRQ9 | IRQ7 |
| Interrupt Service Register2 | 0x1000 0004 | 0xF000 0004 | - | - | - | - | IRQ6 | IRQ5 | IRQ4 | IRQ3 |
| Write Only | | | | | | | | | | |
| Interrupt Clear Register0 | 0x1000 0000 | 0xF000 0000 | - | - | - | - | - | IRQ15 | IDE | IRQ12 |
| Interrupt Clear Register1 | 0x1000 0002 | 0xF000 0002 | - | - | - | - | IRQ11 | IRQ10 | IRQ9 | IRQ7 |
| Interrupt Clear Register2 | 0x1000 0004 | 0xF000 0004 | - | - | - | - | IRQ6 | IRQ5 | IRQ4 | IRQ3 |
| Interrupt Mask Register0 | 0x1000 0008 | 0xF000 0008 | - | - | - | - | - | IRQ15 | IDE | IRQ12 |
| Interrupt Mask Register1 | 0x1000 000A | 0xF000 000A | - | - | - | - | IRQ11 | IRQ10 | IRQ9 | IRQ7 |
| Interrupt Mask Register2 | 0x1000 000C | 0xF000 000C | - | - | - | - | IRQ6 | IRQ5 | IRQ4 | IRQ3 |
| ISA mode Control Register | 0x1000 000E | 0xF000 000E | - | - | - | - | - | ISA reset | ISA mode | - |

Table 6-3 Definition of Each Bit of I/O Control Registers

| Register name | | Value | Description |
|----------------------------|-----------|-------|--|
| Interrupt Service Register | | 1 | IRQx interrupt is occurring |
| | | 0 | IRQx interrupt is not occurring. |
| Interrupt Clear Register | | 1 | IRQx clears interrupt factor. |
| | | 0 | IRQx does not clear interrupt factor. |
| Interrupt Mask Register | | 1 | IRQx masks interrupt input. |
| | | 0 | IRQx does not mask interrupt input. |
| ISA mode Control Register | ISA mode | 1 | High-speed (ISA-incompatible) mode * Normal operation is not guaranteed when this mode is selected. |
| | | 0 | ISA-compatible mode |
| | ISA reset | 1 | Turns ON (H) the RESET signal of PC/104 Bus. |
| | | 0 | Turns OFF (L) the RESET signal of PC/104 Bus. |

6.1.3. Structure of PC/104 Interrupt Controller

The PC/104 interrupt controller is incorporated in the CPLD (XCR3064). Types of interrupt connected to this interrupt controller include IRQ3, 4, 5, 6, 7, 9, 10,11,12, 14 and 15. The conceptual diagram of the interrupt controller is illustrated below.

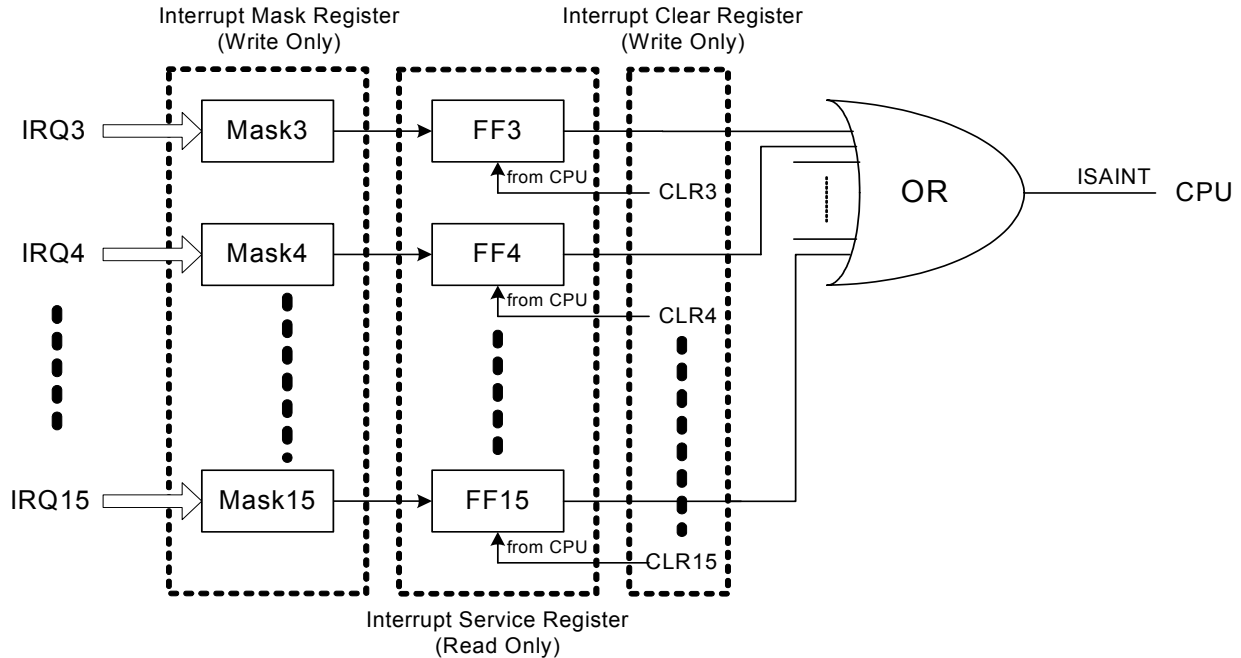


Figure 6-1 Structure of PC/104 Interrupt Controller

The IRQx input from PC/104 is masked by the IMR (Interrupt Mask Register). If the mask bit is "0", the interrupt signal passes through the register without change, while if the mask bit is "1", the interrupt signal is masked.

Interrupt signals that pass through the register are then retained at the FF (flip-flop) that forms the ISR (Interrupt Service Register).

The value held in the ISR is retained until "1" is written to the bit corresponding to the ICR (Interrupt Clear Register).

The OR of the values retained in the ISR is taken and the CPU notified of the interrupts.

6.2. External Interrupts

Connections from outside the board can be made to the external interrupt terminal of the CPU (EP9315) via CON14. Pin-4 of CON14 can be connected to the CPU (EP9315) by shorting JP3. While by shorting JP4, the interrupt output of IC5(S-353xxA) can be sent to outside the board. JP3 and JP4 are set to open at shipment. Both CPU input signals and IC5 output signals are CMOS3.3V voltage level.

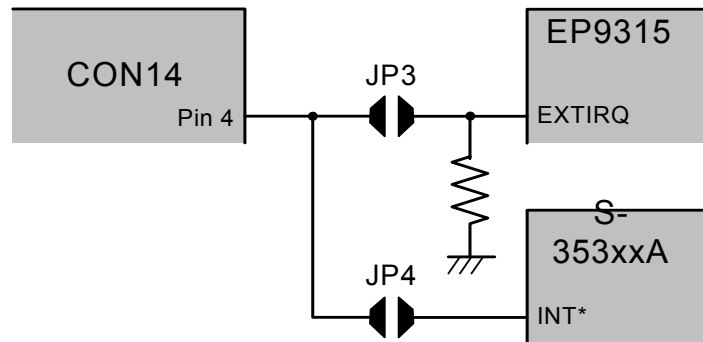


Figure 6-2 EXTIRQ Connections

6.3. LED (D1)

LED (D1) is connected to the PE0/GRLED pin of the CPU (EP9315). After functioning as a status LED when internal ROM is booted, it can be controlled by setting GPIO Port E of EP9315.

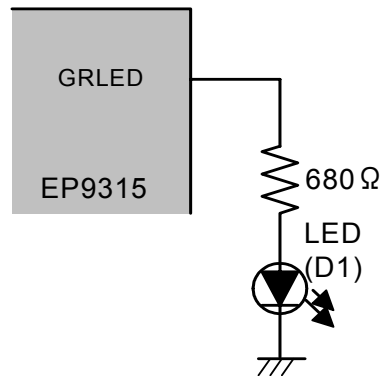


Figure 6-3 LED (D1) Connections

6.4. Calendar Clock (Real Time Clock)

The calendar clock (Real Time Clock: S-3531A or compatible) is connected to the CPU (EP9315) by a 2-wire serial line (GPIO). The CPU end accesses the RTC by controlling parallel port B (PB4, 5: EGPIO12, EGPIO13) in a serial fashion.

During power-off, the RTC can maintain its operation for a certain period of time by the backup of the polyacene capacitor (PAS). An external battery can be connected to maintain the content of the RTC while power is turned off for an extended period of time.

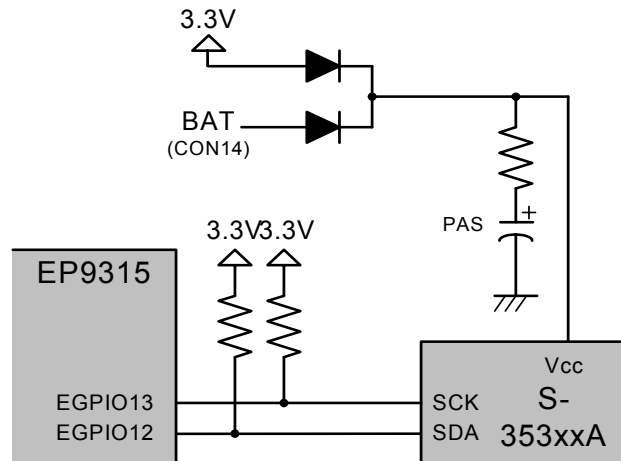


Figure 6-4 Connection of CPU (EP9315) and RTC

6.5. Power Circuit

The power circuit of the Armadillo-9 is shown in Figure 6-5. Be sure not to exceed each current capacity limit when connecting external devices and designing the power supply.

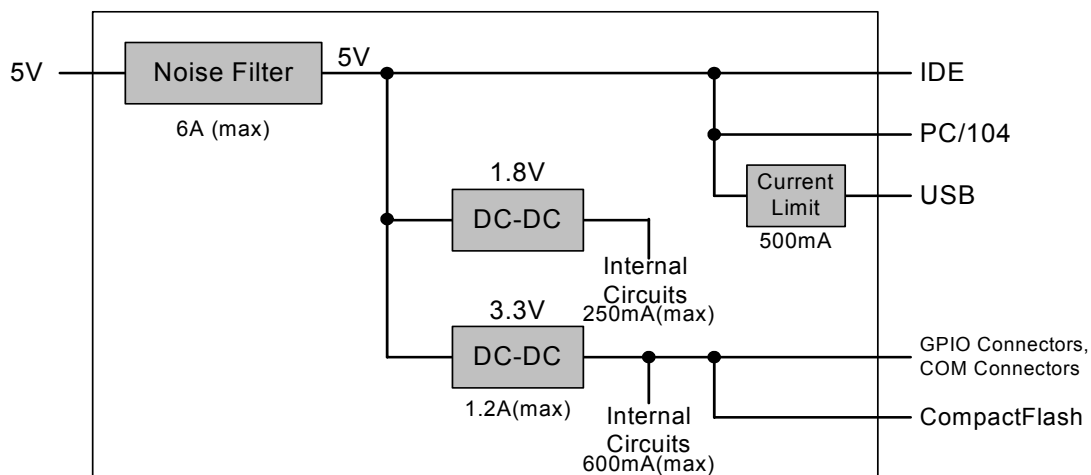
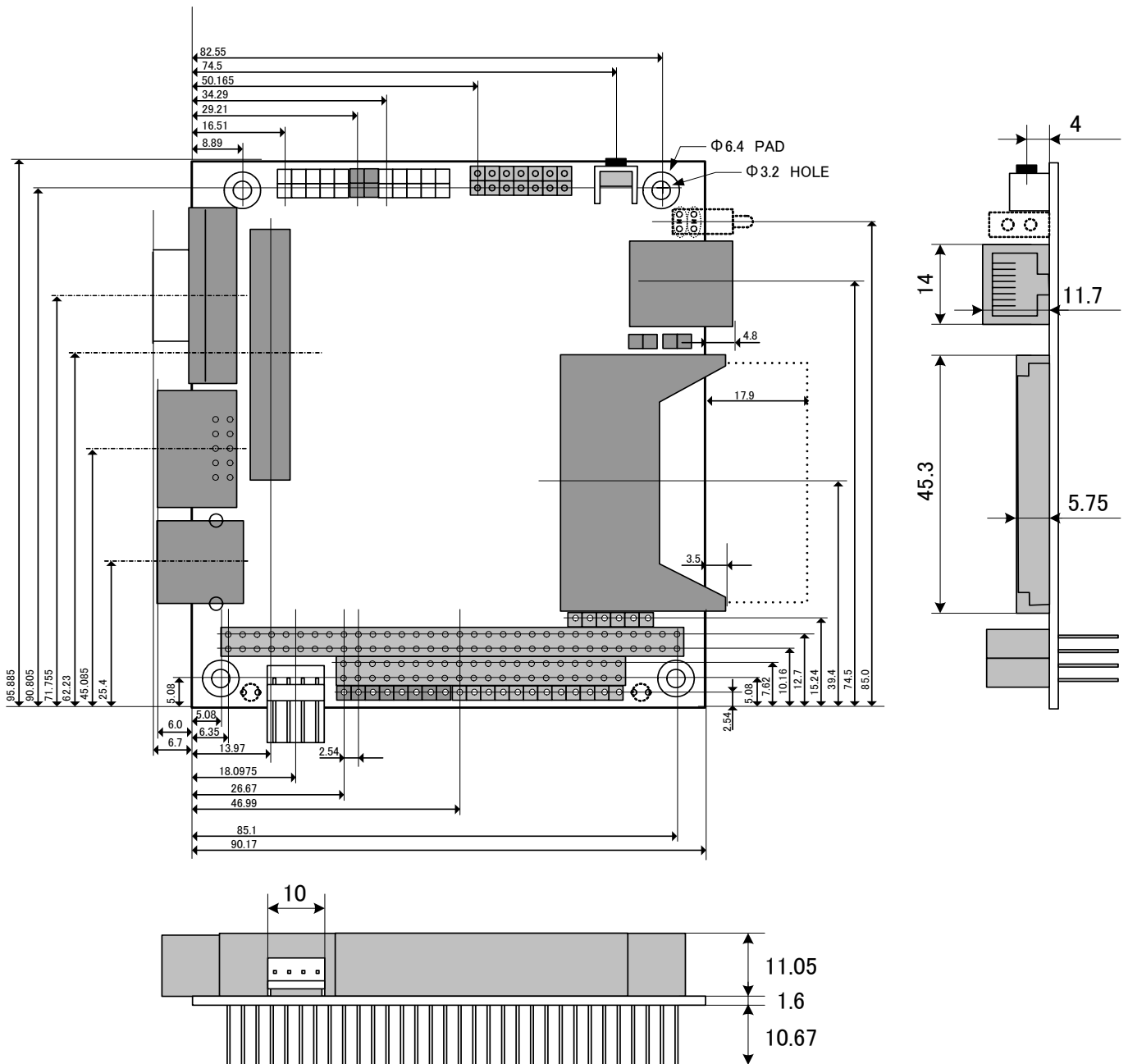


Figure 6-5 Armadillo-9 Power Circuit

7. Board View

Figure 7-1 shows the board view of the Armadillo-9. (Connectors shown in the diagram may not be mounted on some Armadillo-9 models)



(unit: mm)

Figure 7-1 Armadillo-9 Board View

8. Revision History

Revision History

| Version | Date | Description |
|---------|------------|--|
| 1.00 | 2004.12.18 | <ul style="list-style-type: none">• Initial release |
| 1.01 | 2005.2.10 | <ul style="list-style-type: none">• Correction of GPIO value in Table 3-1• Correction of SDRAM memory map Table 4-1• Revision of description of External Interrupts, Section 6.2• Correction of various typographical errors |
| 1.02 | 2005.2.21 | <ul style="list-style-type: none">• Correction to CON1 signal assignment description in Table 5-2• Correction to CON5 signal assignment description in Table 5-7• Correction to table in section 5.7 CON6 (EP9315 JTAG)• Correction to CON10 signal assignment description in Table 5-11• Correction of various typographical errors |

