Freescale Semiconductor
Addendum

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Errata to MCIMX31 and MCIMX31L Applications Processors Reference Manual, Rev. 2.3

This document describes corrections to the *MCIMX31 and MCIMX31L Applications Processors Reference Manual*, Revision 2.3. For convenience, the section number and page number of the errata item in the reference manual are provided.

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4.3.8, 4-116 Add Section 4.3.8.1, “Software-Controllable Signals Register 0 (SCS0),” and Section 4.3.8.2, “Software-Controllable Signals Registers 1–3 (SCS1–SCS3),” as follows:

4.3.8.1 Software-Controllable Signals Register 0 (SCS0)

See Figure 4-199 for an illustration of valid bits in the Software-Controllable Signals Register 0 and Table 4-10 for its field descriptions.

0x5001_C02C (SCS0) Access: Supervisor read/write

	7	6	5	4	3	2	1	0
R	0	SCS[27]	SCS[26]	SCS[25]	SCS[24]	SCS[23]	SCS[22]	SCS[21]
W	LOCK							
Reset	0	0	0	0	0	0	0	0

Figure 4-99. Software Controllable Signals Register 0

Table 4-10. Software Controllable Signals Register 0 Field Descriptions

Field	Description
7 LOCK	Lock this register. This bit is used to lock the contents of this register until the next reset. The intended usage is to have trusted software program the register as desired and lock it before allowing distrusted software to run. This bit is write only; reading this bit returns a zero. 0 The register is not locked; it may be modified. 1 The register is locked; all attempts to modify it are ignored.
6 SCS[27]	Reserved
5 SCS[26]	IPU/ECT DMA Event Source Select. Selects either the IPU or ECT as the DMA event source. 0 IPU (default) 1 ECT
4–0 SCS[24:21]	Reserved

4.3.8.2 Software-Controllable Signals Registers 1–3 (SCS1–SCS3)

See Figure 4-200 through Figure 4-202 for illustrations of valid bits in the Software-Controllable Signals Registers 1–3, and Table 4-11 through Table 4-13 for their field descriptions.

0x5001_C030 (SCS1) Access: Supervisor read/write

	7	6	5	4	3	2	1	0
R	0	SCS[20]	SCS[19]	SCS[18]	SCS[17]	SCS[16]	SCS[15]	SCS[14]
W	LOCK							
Reset	0	0	0	0	0	0	0	0

Figure 4-100. Software Controllable Signals Register 1

Table 4-11. Software Controllable Signals Registers 1

Field	Description
7 LOCK	Lock this register. This bit is used to lock the contents of this register until the next reset. The intended usage is to have trusted software program the register as desired and lock it before allowing distrusted software to run. This bit is write-only; reading this bit returns a zero. 0 The register is not locked; it may be modified. 1 The register is locked; all attempts to modify it are ignored.
6–2 SCS[20:16]	Reserved
1 SCS[15]	Drive strength control ipp_des0 for SDCLK and $\overline{\text{SDCLK}}$. This bit is used in conjunction with ipp_des1(sw_pad_ctl_sdclk[2] in the sw_pad_ctl_sdcke1_sdclk_$\overline{\text{sdclk}}$ register) to determine the drive strength capability of these signals as follows: **Note:** The settings of ipp_des0 is the reverse of the standard settings used in the sw_pad__ctl registers. ipp_dse1* ipp_dse0** Drive Strength 0 1 Standard 0 0 High (default) 1 x Max *sw_pad_ctl_sdclk[2] **SCS[15]
0 SCS[14]	(For revision 2.0 and 2.0.1 silicon) Drive strength control ipp_des0 for SDBA1 and SDBA0. This bit is used in conjunction with SCS[7] in the SCS2 register (functions as ipp_dse1) to determine the drive strength capability of these signals as follows: **Note:** The settings of ipp_des0 is the reverse of the standard settings used in the sw_pad__ctl registers. ipp_dse1* ipp_dse0** Drive Strength 0 1 Standard 0 0 High (default) 1 x Max *SCS[7] **SCS[14]

0x5001_C034 (SCS2) Access: Supervisor read/write

	7	6	5	4	3	2	1	0
R	0	SCS[13]	SCS[12]	SCS[11]	SCS[10]	SCS[9]	SCS[8]	SCS[7]
W	LOCK							
Reset	0	0	0	0	0	0	0	0

Figure 4-101. Software Controllable Signals Register 2

Table 4-12. Software Controllable Signals Registers 2

Field	Description
7 LOCK	Lock this register. This bit is used by the HAB to enable JTAG debugging, assuming that a properly signed command to do so is found and validated by the HAB. The HAB must lock the register before passing control to the OS whether or not JTAG debugging has been enabled. 0 The register is not locked; it may be modified. 1 The register is locked; all attempts to modify it are ignored.
6 SCS[13]	Reserved for future use.
5 SCS[12]	(For revision 2.0 and 2.0.1 silicon) Drive strength control ipp_dse1 for SDQS[3:0]. This bit is used in conjunction with SCS[8] in the SCS2 register (functions as ipp_dse0) to determine the drive strength capability of these signals as follows (note that the definition of ipp_dse0 is reversed from the standard description in the sw_pad_ctl registers): ipp_dse1 (SCS[12]) ipp_dse0 (SCS[8]) drive strength 0 1 standard 0 0 high (default) 1 x max
4 SCS[11]	(For revision 2.0 and 2.0.1 silicon) Drive strength control ipp_dse0 for SDCKE1 and SDCKE0. This bit is used to determine the drive strength capability of these signals as follows (note that the definition of ipp_dse0 is reversed from the standard description in the sw_pad_ctl registers and note that max drive strength is not an option for these signals): ipp_dse0 (SCS[11]) drive strength 1 standard 0 high (default)
3 SCS[10]	Reserved for future use.
2 SCS[9]	(For revision 2.0 and 2.0.1 silicon) Drive strength control ipp_dse0 for SDWE. This bit is used to determine the drive strength capability of these signals as follows (note that the definition of ipp_dse0 is reversed from the standard description in the sw_pad_ctl registers and note that max drive strength is not an option for these signals): ipp_dse0 (SCS[9]) drive strength 1 standard 0 high(default)

Table 4-12. Software Controllable Signals Registers 2 (continued)

Field	Description
1 SCS[8]	(For revision 2.0 and 2.0.1 silicon)) Drive strength control ipp_dse0 for SDQS[3:0]. This bit is used in conjunction with SCS[12] in the SCS2 register (functions as ipp_dse1) to determine the drive strength capability of these signals as follows (note that the definition of ipp_dse0 is reversed from the standard description in the sw_pad_ctl registers): ipp_dse1 (SCS[12]) ipp_dse0 (SCS[8]) drive strength 0 1 standard 0 0 high (default) 1 x max
0 SCS[7]	(For revision 2.0 and 2.0.1 silicon) Drive strength control ipp_dse1 for SDBA1 and SDBA0. This bit is used in conjunction with SCS[14] in the SCS1 register (functions as ipp_dse0) to determine the drive strength capability of these signals as follows (note that the definition of ipp_dse0 is reversed from the standard description in the sw_pad_ctl registers): ipp_dse1 (SCS[7]) ipp_dse0 (SCS[14]) drive strength 0 1 standard 0 0 high (default) 1 x max

0x5001_C038 (SCS3) Access: Supervisor read/write

	7	6	5	4	3	2	1	0
R	0	SCS[6]	SCS[5]	SCS[4]	SCS[3]	SCS[2]	SCS[1]	SCS[0]
W								
Reset	0	0	0	0	0	0	0	0

Figure 4-102. Software Controllable Signals Register 3

Table 4-13. Software Controllable Signals Registers 3

Field	Description
7 LOCK	Lock this register. This bit is used by the HAB to enable JTAG debugging, assuming that a properly signed command to do so is found and validated by the HAB. The HAB must lock the register before passing control to the OS whether or not JTAG debugging has been enabled. 0 The register is not locked; it may be modified. 1 The register is locked; all attempts to modify it are ignored.
6 SCS[6]	MPEG4-EMI throughput improvement 0 INCR bus operation (INCR4 off) 1 INCR4 bus operation on AHB enabled

Table 4-13. Software Controllable Signals Registers 3 (continued)

Field	Description
5–3 SCS[5]–SCS[3]	MSHC2 Programmable Delay Control – These bits determine the amount of delay added in the MSHC2 module between the internal SCLK to the external MSHC2_SCLK pin. SCS[5] SCS[4] SCS[3] delay 0 0 0 0 0 0 1 1 ns 0 1 0 2 ns 1 1 1 7 ns
2–0 SCS[2]–SCS[0]	MSHC1 Programmable Delay Control – These bits determine the amount of delay added in the MSHC1 module between the internal SCLK to the external MSHC1_SCLK pin. SCS[2] SCS[1] SCS[0] delay 0 0 0 0 0 0 1 1 ns 0 1 0 2 ns 1 1 1 7 ns

7.1.1, 7-1 Add “Internal Boot Mode by SD card” to the end of bulleted list.

7.2.1, 7-2 Modify Table 7-1, “System Boot Mode Selection,” as follows:

Table 7-1. System Boot Mode Selection

Inputs BOOT[4:0]	Output Signals Active Device	Boot Address	Comments	Type	Mask
00000	Bootloader USB/UART	32’h0000_0000	Via USB, UART and more	Internal	Rev 2.0 and 2.0.1
00001	8-bit NAND Flash (2 Kbytes per page)	32’h0000_0000	—		Rev 2.0 and 2.0.1
00010	8-bit NAND Flash (512 bytes per page)	32’h0000_0000	—		Rev 2.0 and 2.0.1
00011	16-bit NAND Flash (2 Kbytes per page)	32’h0000_0000	—		Rev 2.0 and 2.0.1
00100	16-bit NAND Flash (512 bytes per page)	32’h0000_0000	—		Rev 2.0 and 2.0.1
00101	16-bit CS0 at D[15:0]	32’h0000_0000	—		Rev 2.0 and 2.0.1
00110	Bootloader Serial USB/UART	32’h0000_0000	Via USB or UART		Rev 2.0.1
00111	MMC_SD (2 Kbytes)	32’h0000_0000	SD Card		Rev 2.0.1
01000	Bootloader Atlas-Serial USB/UART	32’h0000_0000	Via USB or UART		Rev 2.0.1
01001	M-Systems Disk On Chip (2 Kbytes)	32’h0000_0000	MDOC FLASH		Rev 2.0 and 2.0.1
01001–01111	Reserved	32’h0000_0000	Acts as bootloader UART/USB mode		Rev 2.0 and 2.0.1

Table 7-1. System Boot Mode Selection (continued)

Inputs BOOT[4:0]	Output Signals Active Device	Boot Address	Comments	Type	Mask
10000	8-bit NAND Flash (2 Kbytes per page)	NANDFC base	—	External	Rev 2.0 and 2.0.1
10001	8-bit NAND Flash (512 bytes per page)	NANDFC base	—		Rev 2.0 and 2.0.1
10010	16-bit NAND Flash (2 Kbytes per page)	NANDFC base	—		Rev 2.0 and 2.0.1
10011	16-bit NAND (512 bytes per page)	NANDFC base	—		Rev 2.0 and 2.0.1
10100	16-bit CS0 at D[15:0]	EMI base	—		Rev 2.0 and 2.0.1
10101–10110	Reserved	External Memory	Acts as 16-bit CS0-External		Rev 2.0 and 2.0.1
10111	Reserved	—	Reserved for Manufacturing and Test	Internal	Rev 2.0 and 2.0.1
11xxx	Reserved	—	Manufacturing and Test	—	Rev 2.0 and 2.0.1

7.6, 7-4 Add Section 7.6, “MMC/SD Card,” as follows:

7.6 MMC/SD Card

The access to the card is done through SDHC on Port 1 and 1-bit mode. The internal ROM reads the first 2 Kbytes from the card and copies it to the base address of IRAM.

Figure 7-3 shows the SD Boot flow (including HighCapacity) starting from the MMC/SD Boot entry point.

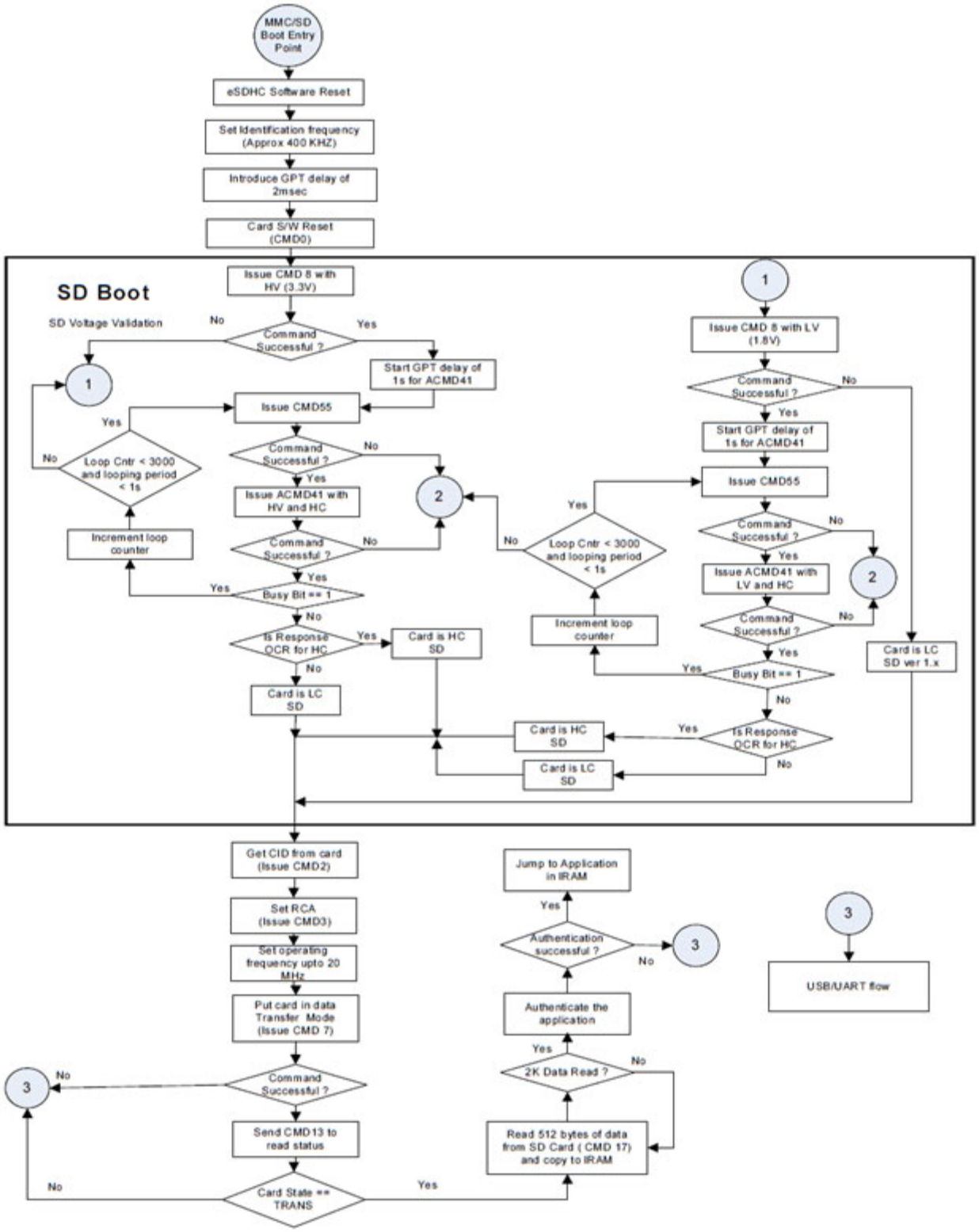

Figure 7-3. SD Boot Flow (including HighCapacity) Starting from MMC/SD Boot Entry Point

Figure 7-4 shows the MMC Boot flow (including HighCapacity).

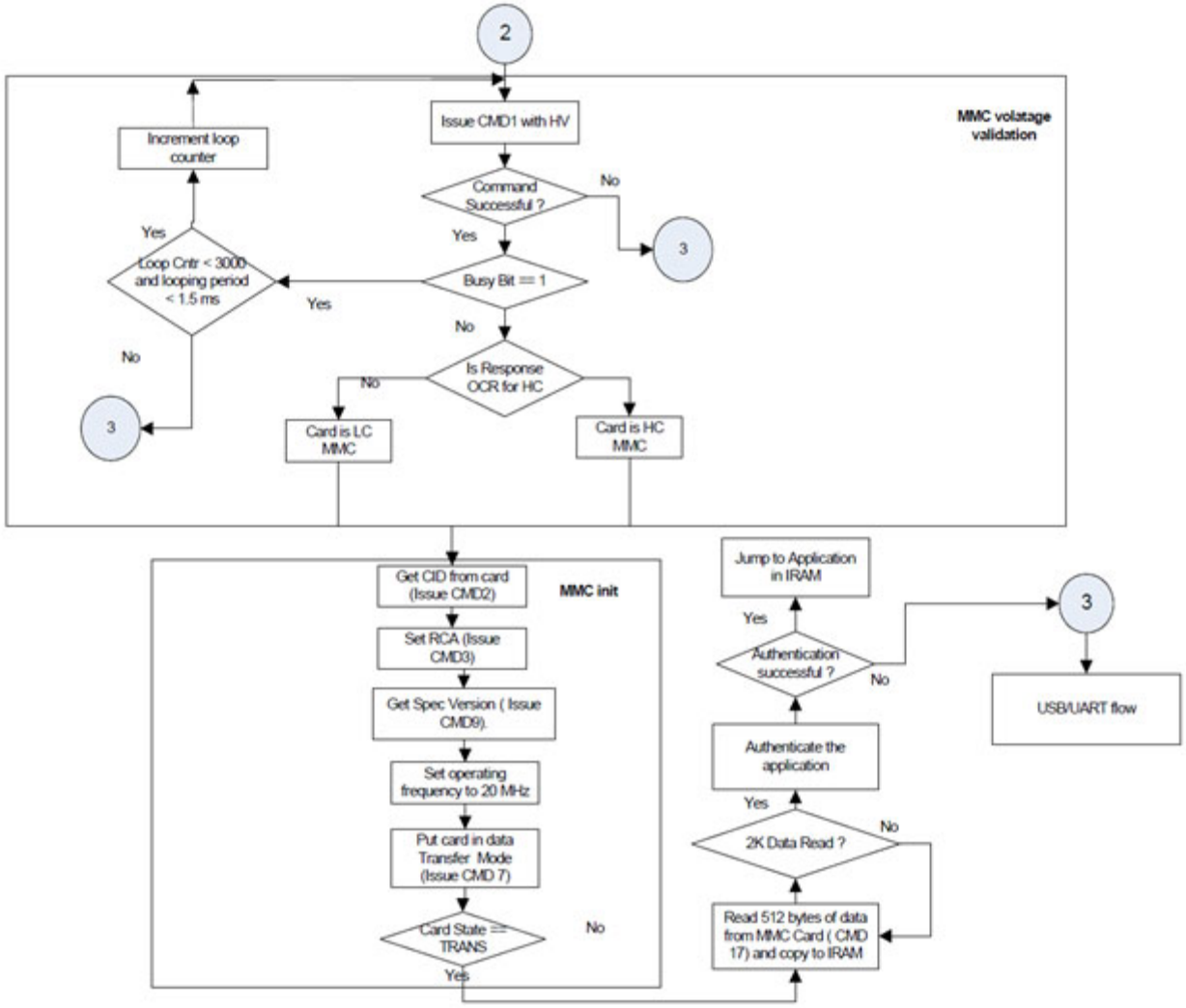

Figure 7-4. MMC Boot Flow (Including HighCapacity)

13.2.2.1, 13-3 Add 2.0/2.0.1 revision rows and change “Device Marking” to “Device Mask” in column headings in Table 13-2, “SILICON_REV Settings,” as follows:

Table 13-2. SILICON_REV Settings

SREV	Device	Silicon Revision	Device Mask Wafer Fab 1	Device Mask Wafer Fab 2
0x00	i.MX31 and i.MX31L	1.0	L38W	—
0x10	i.MX31	1.1	2L38W	—
0x11	i.MX31L	1.1	2L38W	—

Table 13-2. SILICON_REV Settings (continued)

SREV	Device	Silicon Revision	Device Mask Wafer Fab 1	Device Mask Wafer Fab 2
0x12	i.MX31	1.15	2L38W 3L38W[1]	—
0x13	i.MX31L	1.15	2L38W 3L38W[1]	—
0x14	i.MX31	1.2	3L38W[2]	M45G
0x15	i.MX31L	1.2	3L38W[3]	M45G
0x28	i.MX31	2.0/2.0.1	—	M91E
0x29	i.MX31L	2.0/2.0.1	—	M91E

[1] Misidentified device. IC stamped 3L38W, SREV register reads correct value: 2L38W. The device marking has the initial characters MCIMX31.

[2] Non-production part used for population of ADS boards. The device marking has the initial characters PCIMX31.

[3] Non-production part and is not available. The device marking has the initial characters PCIMX31.

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