i.MX31 and i.MX31L Multimedia Applications Processors

1   Introduction

The MCIMX31 (i.MX31) and MCIMX31L (i.MX31L) multimedia applications processors represent Freescale Semiconductor's latest achievement in multimedia integrated applications processors that are part of a growing family of multimedia-focused products offering high performance processing optimized for lowest power consumption. The i.MX31 and i.MX31L processors feature Freescale's advanced and power-efficient implementation of the ARM1136JF-S™ core, which operates at speeds starting at 532 MHz.

Unless otherwise specified, the material in this product brief is applicable to both the i.MX31 and i.MX31L processors. Features include the following:

*   **Smart Speed Technology**—The heart of the i.MX31 and i.MX31L processors is a level of power management throughout the ICs that allow the rich suite of multimedia features and peripherals to achieve minimum system power consumption in both active and various low-power modes. Smart Speed Technology

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enables the designer to deliver a feature-rich product that requires levels of power that are far less than typical industry expectations.

- **Multimedia Powerhouse**—The multimedia performances of the i.MX31 and i.MX31L processors are each boosted by a multi-level cache system and further enhanced by an MPEG-4 hardware accelerator that provides MPEG-4 SP encoding up to VGA resolution at 30 fps, as well as an Autonomous Image Processing Unit, Vector Floating Point (VFP11) co-processor, and a programmable SDMA controller.

- **Powerful Graphics Acceleration** (not available in the i.MX31L)—3D graphics are the key to mobile game designs. The i.MX31 processor delivers an integrated 3D Graphics Processing Unit (GPU) that provides an incredible 0.8–0.9 MTri/sec (double textured, bi-linear, Gouraud shaded) at about 100 Mpix/sec (effective).

- **Interface Flexibility**—The i.MX31 and i.MX31L processors' interface support connection to all popular types of external memories—DDR, SDRAM, NAND Flash, NOR Flash, SRAM, and MDOC. Designers seeking to provide products that deliver a rich multimedia experience will find a full suite of on-chip peripherals: LCD controller and CMOS sensor interface, High Speed USB On-The-Go, and two USB hosts, a multiple expansion card, and serial interfaces. There is even an ATA hard disk controller in each processor. An important design goal of the i.MX31 and i.MX31L processors is their rich and flexible connectivity support to ensure that any system configuration can be developed quickly and at minimum material cost.

- **Increased Security**—Because the need for advanced security for mobile devices continues to increase, the i.MX31 and i.MX31L processors deliver hardware-enabled security features allowing secure e-commerce, digital rights management (DRM), information encryption, secure boot, and secure software downloads.

Regardless of whether you are designing a smartphone, PDA, gaming console, or other portable device, the i.MX31 and i.MX31L processors provide your design with the power and flexibility necessary for today's competitive marketplace.

2 Features

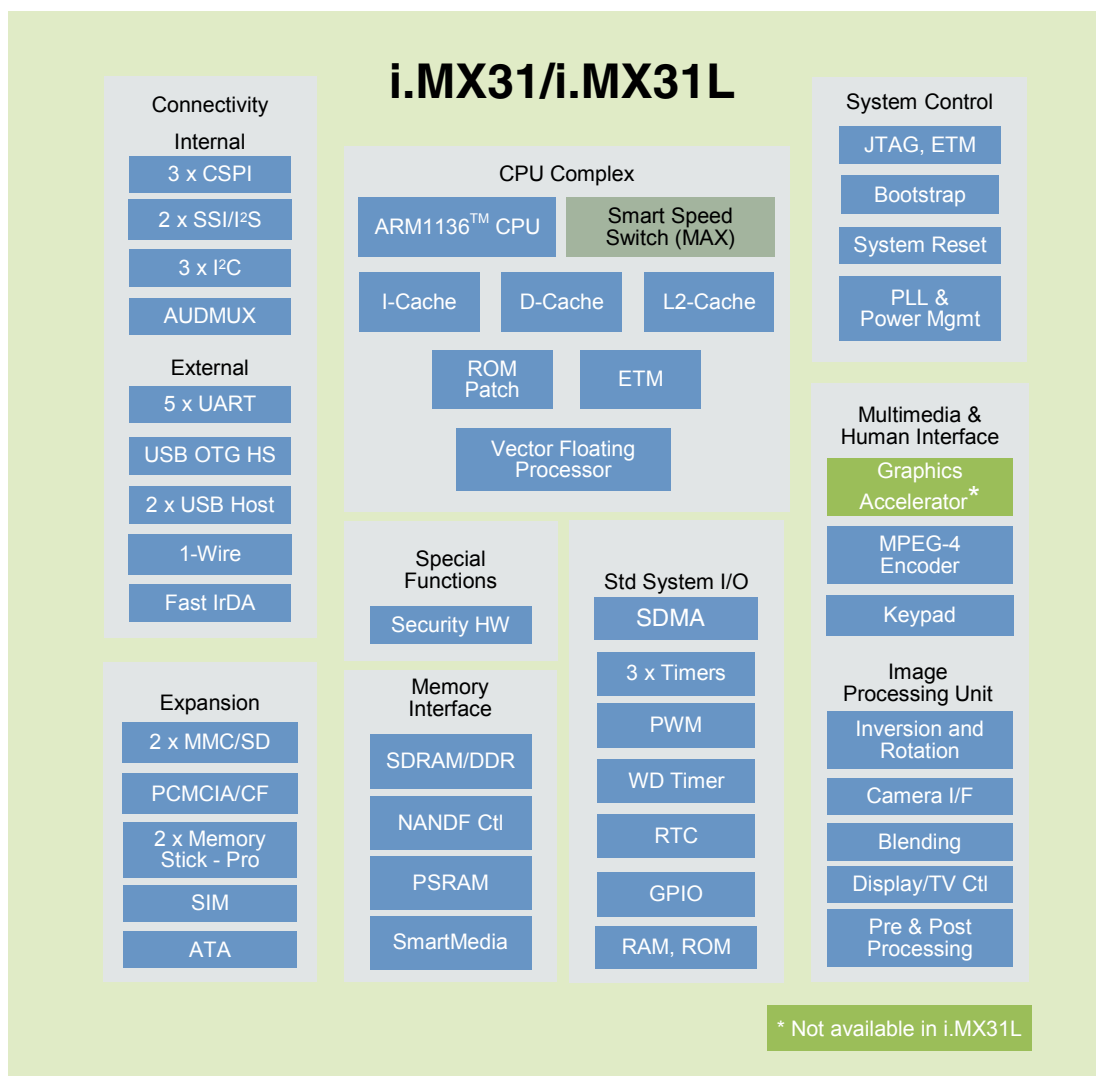illustrates the functional modules of the i.MX31 and i.MX31L processors.

Figure 1. i.MX31 and i.MX31L Functional Block Diagram

2.1 ARM11™ Platform

The ARM11™ platform consists of the ARM1136JF-S processor, a level 2 (L2) cache system, 6 × 5 multi-layer AHB 2.v6 Smart Speed Crossbar Switch (MAX), L2 memory system, and an ARM11 vectored interrupt controller (AVIC).

In addition, the ARM11 platform contains the Embedded Trace Kit™ (ETK) from ARM Ltd. These modules consist of the Embedded Trace Macrocell™ (ETM™), the Embedded Trace Buffer™ (ETB™), and the Cross Trigger Interface (CTI) module.

2.1.1 ARM1136JF-S Platform Modules

The modules that are used in the ARM1136JF-S Platform include the following:

- **The ARM1136JF-S CPU core**—Based on the ARM® v6 architecture. It supports the ARM Thumb® instruction set, Jazelle® technology to enable direct execution of Java™ byte codes, and a range of SIMD DSP instructions that operate on 16-bit or 8-bit data values in 32-bit registers.

- **The VFP11 coprocessor**—An ARM enhanced IEEE® 754 numeric coprocessor that can be used to support and enhance 3D graphics, gaming, high resolution audio, Java, and other general-purpose applications.

- **A Multi-Level Cache system**—Consisting of a powerful L2 Cache Controller, 128 Kbytes unified L2 cache memory and L2 cache monitor. The L2 cache controller (L2CC) module has been optimized by ARM to Freescale's specifications. The L1 cache provides 16 Kbytes for instruction and 16 Kbytes for data.

- **Multi-Layer 6 × 5 AHB Smart Speed Crossbar Switch (MAX)**—The L2CC master ports, the off-platform alternate bus masters, and the ARM11 processor's peripheral AHB arbitrate for memory and peripherals via a 6 × 5 Multi-Layer AHB crossbar switch. The design of the MAX allows concurrent transactions to proceed from any slave port to any master port. That is, it is possible for five MAX slave ports to be active at the same time as a result of five independent master requests.

  If a particular slave port is simultaneously requested by more than one master port, arbitration logic exists in the MAX to allow the higher priority master port to be granted access to the slave, while stalling the other requestor(s) until that transaction is complete. The slave port arbitration schemes supported are fixed, programmable fixed, round-robin, and programmable default parking.

- **L2 Memory System**—The embedded 16 Kbytes SRAM and 32 Kbytes ROM are accessible by the ARM CPU and the SDMA controller. ROM holds the High Assurance Boot code.

2.2 Smart Power Management by Design

The i.MX31 and i.MX31L processors' power management system includes an effective combination of established and ground-breaking (patent pending) technologies to ensure the following design goals are achieved:

- The operation of the IC is well balanced, providing the optimum trade-off between performance and power consumption.

- Power is expended only when it is actually required by an application.

- When power is required, the minimum amount of power is used to complete the application.

There is always a trade-off between the potential performance that can be achieved and the leakage current that is unavoidable to obtain a high level of performance because higher performance requires solid state devices with increased leakage. To ensure the best possible performance trade-off, the i.MX31 and i.MX31L processors are manufactured using a 90-nm, low-power process to ensure minimum power dissipation by leakage. At the same time, dual Vt technology is used to incorporate the high performance transistors in places where the performance is critical, therefore, producing the best overall trade-off between performance and leakage.

The following techniques are used to reduce static power consumption:
- Active Well Bias (AWB)
- Power gating
- A variety of low-power modes
- Special techniques for fast wake-up times from low-power modes

The following techniques are used to reduce dynamic power consumption:
- Dynamic process and temperature compensation
- Automatic dynamic voltage frequency scaling
- Low-power clocking scheme

2.3   External Memory Interface (EMI)

To allow the maximum number of potential designs, the External Memory Interface of the i.MX31 and i.MX31L processors provide support for the following memory types:
- SRAM, NOR Flash and PSRAM—32/16-bit, Disk-On-Chip
- SDRAM, SyncFlash™, VSyncFlash™—133 MHz, 32/16-bit
- DDR—266 MHz, 32/16-bit
- NAND Flash and SmartMedia (dedicated 8-bit, shared 16-bit)

2.4   Smart Multimedia

Multimedia is one of the most important features for today's mobile devices. The i.MX31 and i.MX31L processors' provide multimedia hardware acceleration for a wide variety of multimedia applications at performance levels that are the equivalent of ARM11 processor performance of more than 3 GHz. The optimized hardware acceleration enables some typical applications to operate without ARM CPU involvement—for example, the viewfinder.

The i.MX31 and i.MX31L processors' smart multimedia design enables the following:
- Simultaneous MPEG-4 Simple Profile (SP) video encoding and decoding.
- Real-time video decode in any of the following advanced formats:
  — MPEG-4 Simple Profile (SP)
  — H.264
  — WMV (Windows Media™ Video)
  — RV (RealVideo™)
  — MPEG-2
  — DiVX
- Video and image data pre/post-processing (resizing, color conversion, filtering) that is fully hardware accelerated.

2.4.1 Video Applications

The i.MX31 and i.MX31L processors are optimized to support a variety of video applications. Figure 2 on page 6 describes the video processing chain and its implementation.
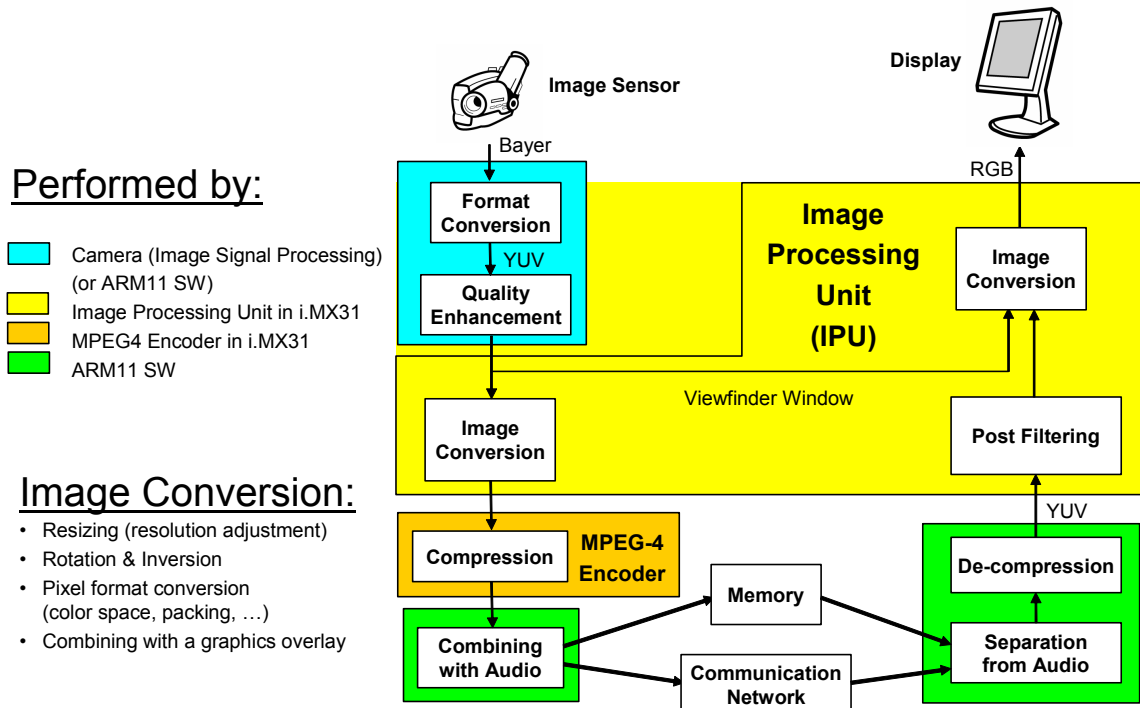

Figure 2. Video Processing Chain

The video implementation in the i.MX31 and i.MX31L processors is a result of a smart trade-off between performance and flexibility. The following points describe some of the video performance features:

- **Image processing**—The processing required for a camera preview function is performed fully in hardware, allowing the CPU to be powered-down in this stage.

- **Encoding**—MPEG-4 SP and the H.263 baseline formats are fully hardware accelerated, supporting resolutions up to VGA at 30 fps. As a result, a high degree of power efficiency is achieved, and the CPU is freed to perform other tasks. Encoding for other video standards are achieved using software implementation.

- **Decoding**—Based on a mixture of software and hardware, this implementation provides the greatest flexibility to support a variety of algorithms and future extensions. A sufficient software optimization level may be achieved using the advanced ARM11 instruction set and multi-level cache system. For MPEG-4, the post-filtering (de-blocking and de-ringing) is accelerated by IPU hardware, resulting in a 75% load reduction on the ARM11 core. For H.264 baseline format—the most processing-intensive format—the deblocking filter is also performed in hardware providing a 30% acceleration improvement The powerful ARM11 processor (including its 2-level cache system) provides the flexibility to decode at a high rate any currently relevant formats (up to HVGA @ 30 fps), as well as possible future extensions.

Figure 3 (preview), Figure 4 (capture), and Figure 5 (playback) illustrate system views of the video process using the MPEG-4 SP format. (The flow for other formats is very similar.)

2.4.2 MPEG-4 Encoding Accelerator

The video encoding hardware accelerator of the i.MX31 and i.MX31L processors support MPEG-4 Simple Profile (all levels) and H.263 Baseline. They enable pixel rates up to VGA at 30 fps and compressed bit rate up to 4 Mbps.
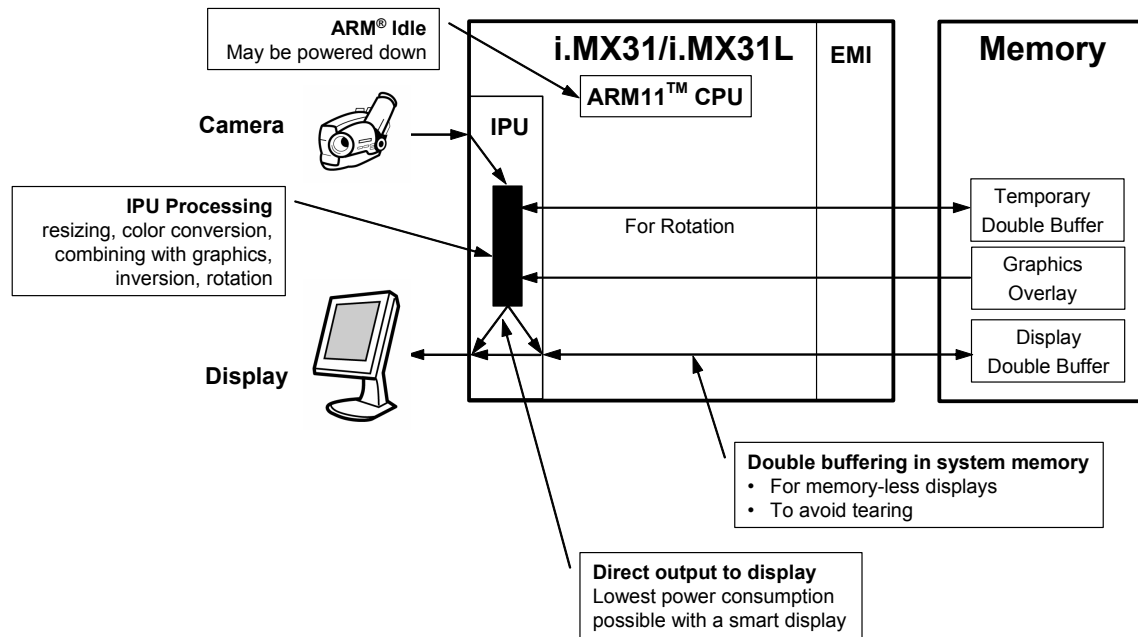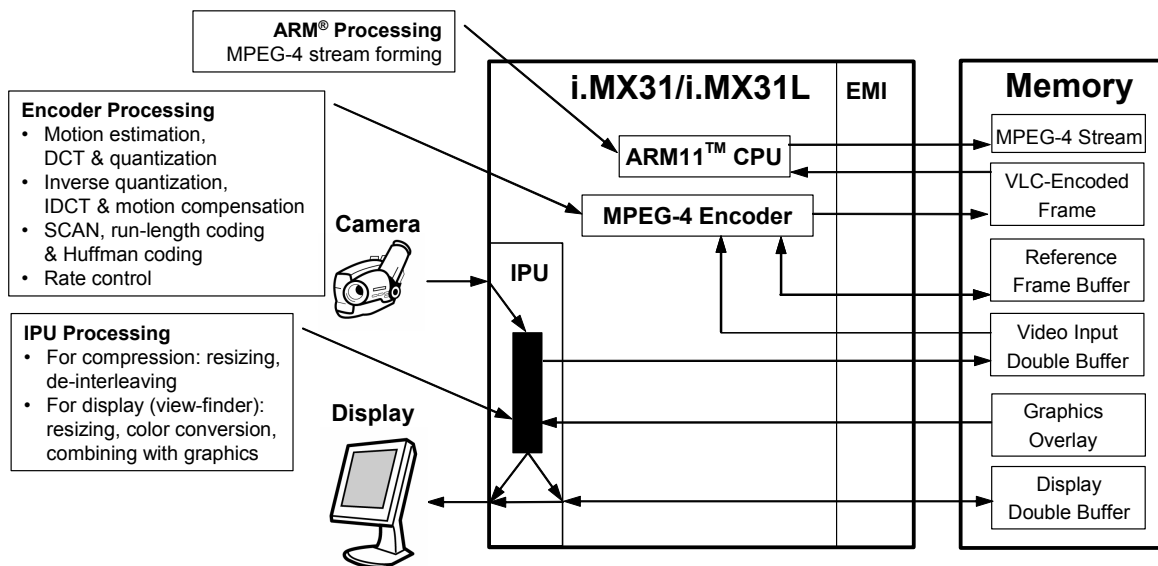

Figure 3. Camera Preview—Data Flow

Figure 4. MPEG-4 SP Video Capturing—Data Flow

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ARM® Processing
• Huffman decoding, run-length decoding and inverse scan
• Inverse quantization, IDCT & motion compensation

i.MX31/i.MX31L **EMI** **Memory**

ARM11™ CPU

MPEG-4 Stream

Reference Frame Buffer

Camera

IPU

MPEG-4 Encoder

IPU Processing
De-blocking, de-ringing, resizing, color conversion, combining with graphics

Video Input Double Buffer

Graphics Overlay

Display

Display Double Buffer

Figure 5. MPEG-4 SP Video Play-Back—Data Flow

2.5   2D/3D Graphics Support

The i.MX31 processor includes the Graphics Processing Unit (GPU) to provide hardware acceleration for 2D and 3D graphics algorithms. The acceleration is enough to run desktop quality interactive graphics applications on displays with the screen resolution of VGA and above and color representation up to 32 bits per pixel. The GPU uses the ARM MBX R-S graphics accelerator. shows the GPU high level block diagram and processing data flow.

NOTE

The Graphics Processing Unit (GPU) is not available in the i.MX31L processor.
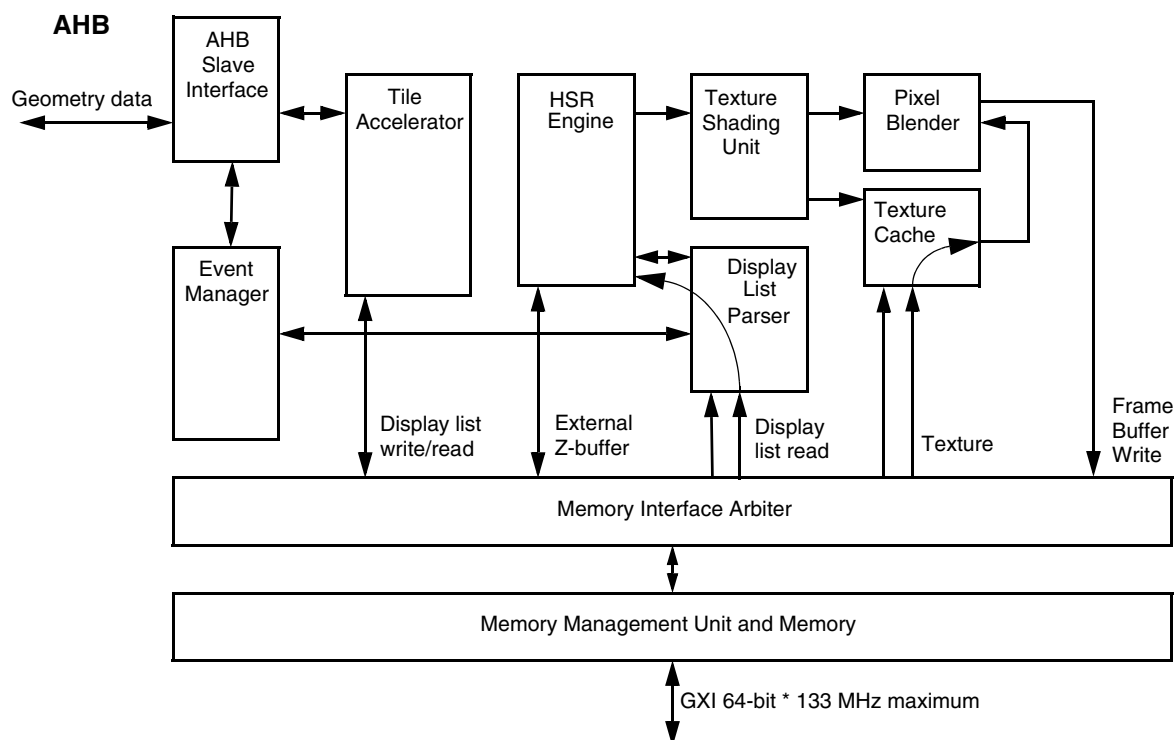
Figure 6. GPU Block Diagram and Data Flow

2.6   Display Port

The display port of the i.MX31 and i.MX31L processors provide the ability to connect to a wide variety of popular display devices:

- RAM-less LCD panels—up to 40 Mpix/sec (for example, SVGA @ 80 fps), 262k colors Results are dependent on end application.
- LCD panels with integrated frame buffer—up to 1024×1024, 14M colors. Results are dependent on end application.
- TV encoders

The i.MX31 and i.MX31L processors' display ports enable simultaneous connectivity of up to two displays —an LCD without memory and a TV encoder, as well as provides connectivity to three interface types:

- Synchronous parallel (18-bit)
- Asynchronous parallel (18-bit)
- Synchronous Serial (SPI-like) at a bus rate of up to 100 MHz

2.7   Sensor Port

The sensor port provides a connection to either one or two image sensors, of which only one sensor can be active at any given time. The sensor port supports direct parallel interface to either CMOS or CCD sensor controllers using parallel interface with widths of 12-bit, 10-bit, 8-bit, or 4-bit wide and at data bus rates

up to 60 MHz. The sensor port may be configured to perform output of a still image to a non-contiguous memory buffer, enabling efficient memory use under open OS.

2.8   System Connectivity

Figure 7 shows an example of the i.MX31 and i.MX31L processors' connectivity with a rich set of external devices.
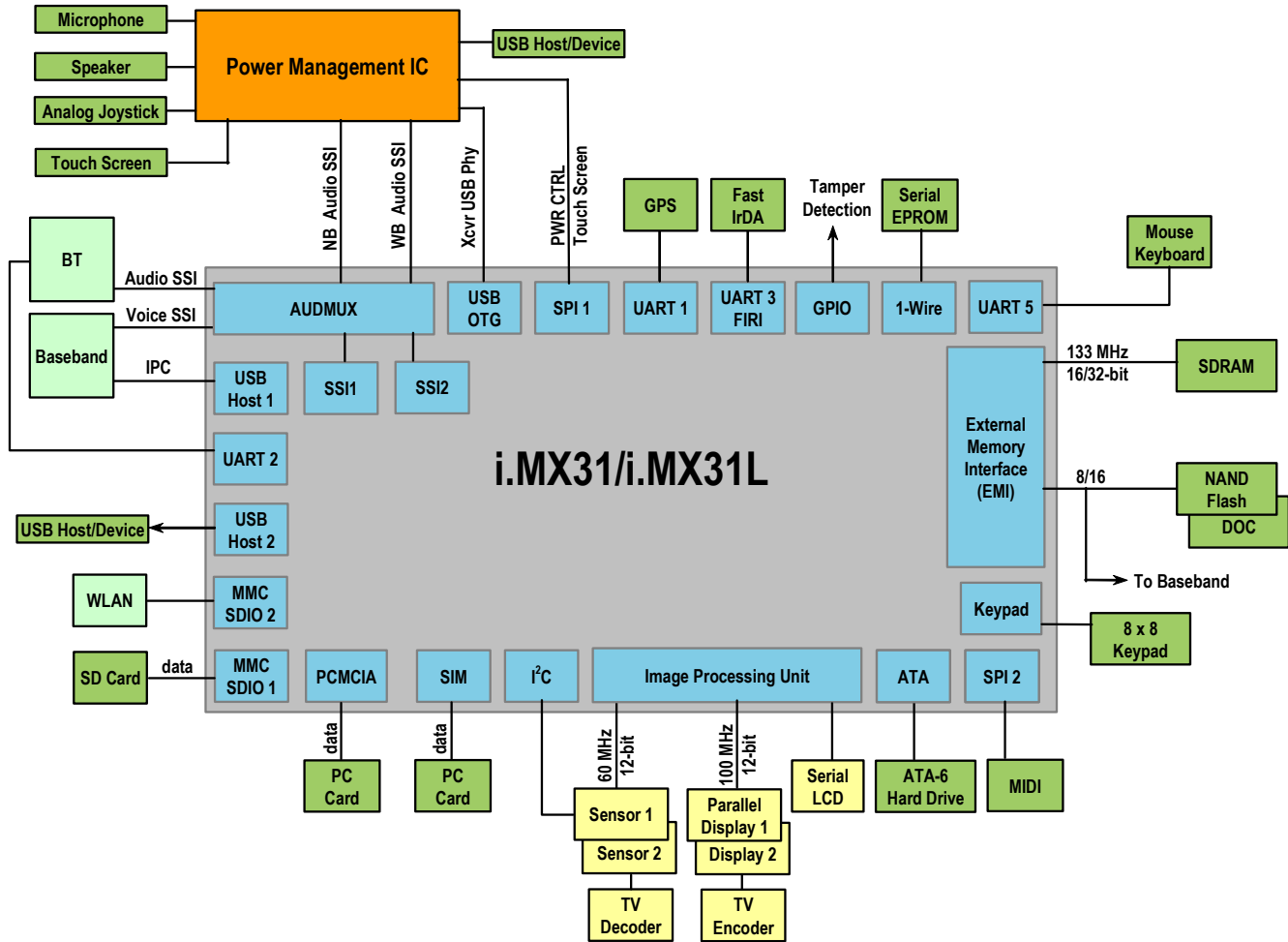
Figure 7. i.MX31 and i.MX31L Connectivity Example

2.8.1   High Speed USB 2.0 Interface

The i.MX31 and i.MX31L processors each support three independent USB 2.0 ports, two of which support high speed (HS) operation:

- OTG—High speed (480 Mbps)
- Host 1—High speed (480 Mbps)
- Host 2—Full speed (12 Mbps)

The ability of the i.MX31 and i.MX31L processors to provide an HS USB connection allows you to deliver a product that can download 500 Mbytes of video in 15 seconds, in contrast to nearly 10 minutes using full speed. The USB connectivity of either i.MX31 or i.MX31L processor provides extremely fast synchronization with a PC or between two devices. Any of the USB ports may be used for transceiver-free connection, or for external transceiver-based connection.

The USB OTG port can connect to a PC as either a device or as a host to any of the following peripherals: keyboard, printer, mouse, speakers, storage device, digital camera, and so on. It supports 16 endpoints for each host and device.

USB Host 1 is typically connected to dedicated ICs that support WLAN, Bluetooth™ wireless technology, and GPS. Host 1 supports 16 endpoints. USB Host 2 is typically used to connect to ICs for baseband or WLAN, Bluetooth wireless technology, or GPS. Host 2 supports 4 endpoints.

2.8.2   Audio Flexible Interconnect

The Digital Audio Mux (AUDMUX) provides a programmable interconnect fabric for voice, audio, and synchronous data routing between each i.MX31 and i.MX31L processors' SSI modules and external SSI, audio, and voice codecs. The AUDMUX is designed so that resource configurations do not need to be hard-wired, but instead, can be shared in many different configurations. The AUDMUX interconnections allow multiple simultaneous separate audio/voice/data flows between the ports in a point-to-point or point-to-multipoint configuration(s).

In a typical scenario, the AUDMUX and two SSI/I^{2}S modules provide interfaces to the Serial Audio Port of the cellular baseband (BB) processor, narrowband (NB), and wideband (WB) audio ports of the external audio AD/DA and the audio port of the Bluetooth wireless technology on-board peripheral. See Figure 8.
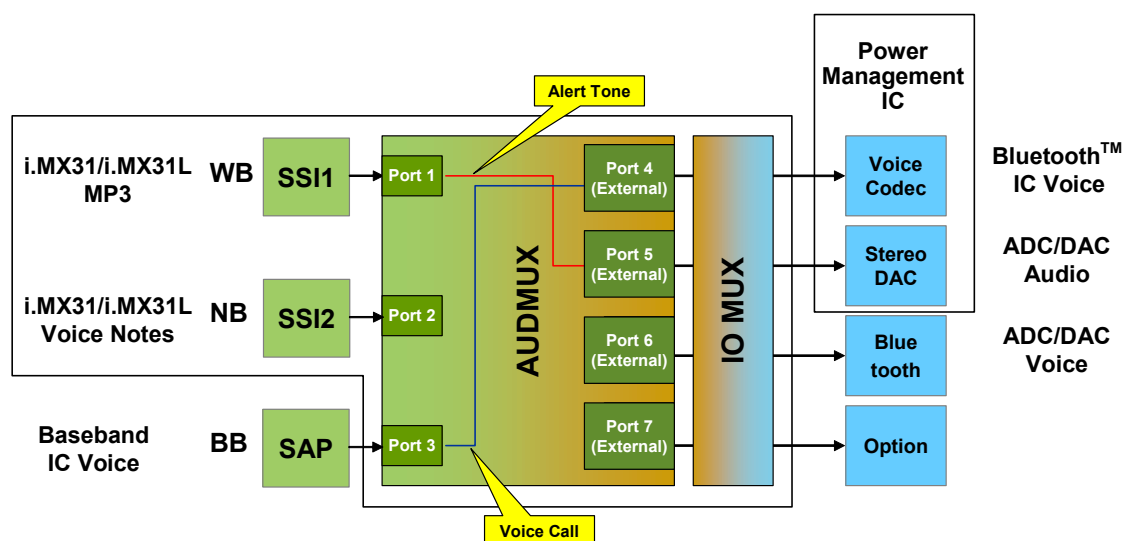

Figure 8. Typical AUDMUX Application

2.9   Security Features

Not only do the i.MX31 and i.MX31L processors offer a wide assortment of security features, but these features are robust and offer a high degree of protection for security. The i.MX31 and i.MX31L processors'

security architecture is based on efficient system partitioning between software and hardware implementations.

The following security features are implemented:

- MMU (Memory Management Unit)
- Security Controller (SCC), including *Secure RAM* and *Security Monitor*
- Random Number Generator Accelerator (RNGA)
- Secure JTAG controller (with optional JTAG disabling)
- Universal Unique Identification
- Real Time Integrity Checker (RTIC), Including SHA-1 accelerator
- High Assurance Boot (HAB)
- Tamper Detection

These security features are intended to address the following concerns:

- Service carriers concerns of portable device cloning and theft of services
- OS and vendor SW authentication
- Secure mobile communications and transactions
- Secure video conference call
- Secure M-commerce
- Digital rights management (DRM)
- Defense against physical tampering

2.9.1   Security Controller (SCC)

The SCC provides a series of tools to the product developer to allow sensitive data (such as keys, certificates, account information, and so on) to be protected using storage from the main processor. The SCC is setup so that information is encrypted using a hardware block that only that specific processor can then decrypt.

2.9.2   Secure JTAG Controller (SJC)

JTAG manipulation is one of the known methods hackers use to bypass security measures and gain control over a system. The Secure JTAG Controller regulates JTAG access by allowing only debugging tools with the appropriate key to access the JTAG port.

2.9.3   Run-Time Integrity Checker (RTIC)

The Run-Time Integrity Checker (RTIC) ensures the integrity of the peripheral memory contents and also assists with boot authentication. The RTIC has the ability to verify the memory contents during system boot and during run-time execution. If the memory contents at runtime fail to match the hash signature, an error in the security monitor is triggered.

2.9.4 Random Number Generator Accelerator (RNGA)

The RNGA (Random Number Generator Accelerator) module is a digital integrated circuit capable of generating 32-bit random numbers. It is designed to comply with FIPS-140 (Federal Information Processing Standard) standards for randomness and non-determinism. The configuration of the shift registers ensures statistically good data—that is, data that appears random.

2.9.5 Tamper Detection

The Tamper Detection system provides evidence of any physical attempt to remove the device's cover. This solution involves an external hardware tamper detector connected to a GPIO pin of the i.MX31 and i.MX31L processors with capability to generate an ARM interrupt. The same GPIO pin is connected to the SCC module. When a tamper attempt is detected, the GPIO tamper detection pin signals the SCC, which resets the Secure RAM to zero and transits into failure mode. In addition, the ARM interrupt request is generated.

2.9.6 High Assurance Boot (HAB)

The system boot flow, defined in the i.MX31 and i.MX31L processors, controls and assures that the system boots up in a predefined secure path and ensures that the software in Flash ROM runs on the system for which it was intended. This helps to prevent unauthorized modification to the trusted OS. This turns the Flash ROM into tamper-evident memory, protecting against unauthorized key(s) extraction or hacking program downloads as well as viruses. The flow makes use of security hardware and software components to protect flash image, and to create a well-bonded, secure-based platform for the core and other functional modules.

External Boot is supported as one of the boot modes. In general, this may be interpreted as a security hazard. Using external boot, it is possible to run code without requiring it to pass the authentication checks. Sometimes, however, external boot is required in debug and development processes. The External Boot option may be disabled if the corresponding on-chip E-Fuse (Electrical Fuse) is blown.

2.10 Smart Direct Memory Access (SDMA)

The Smart Direct Memory Access (SDMA) controller maximizes the system's performance by relieving the ARM core of the task of bulk data transfer from memory to memory or between memory and on-chip peripherals. The advantage of the SDMA controller is its dynamic routing capability and that it can perform numerous tasks simultaneously, based on the DMA channel's descriptors. Application Processor Operating System software drivers can make extensive use of DMA channels to minimize software overhead and transfer latencies.

2.11 Standard System Functions

The i.MX31 and i.MX31L processors each contain the essential system modules necessary to ensure the designer has the maximum flexibility in programming and choice of peripherals.

2.11.1   Keypad

The keypad is designed to simplify the software task of scanning an 8×8 keypad matrix. With appropriate software support, the module is capable of detecting, debouncing, and decoding one or two keys pressed simultaneously in the keypad. Even while the processor is in low-power mode, the keypad can generate a CPU interrupt upon key press.

2.11.2   Timers

The i.MX31 and i.MX31L processors each provide a rich and varied assortment of timers to meet the program and event timing needs of the designer.

- **Real-Time Clock (RTC)**—Maintains the system clock, and provides stopwatch, alarm, and interrupt functions.
- **Enhanced Periodic Interrupt Timer (EPIT)**—Two EPITs provide precise interrupts at regular intervals with minimal processor intervention.
- **General Purpose Timer (GPT)**—Measures intervals or generate periodic outputs.
- **Watchdog Timer (WDOG)**—Protects the system from unexpected events or programming errors. The WDOG timer module also generates a system reset using a software write to the Watchdog Control Register (WCR), a detection of a clock monitor event, an external reset, an external JTAG reset signal, or an occurrence of a power-on reset.

2.11.3   Pulse Width Modulation (PWM) Module

The pulse width modulator (PWM) is based on a 16-bit counter and is optimized to generate sound from stored sample audio files. The PWM can also generate tones. It uses 16-bit resolution and a 4×16 data FIFO to generate sound.

2.11.4   Serial Interfaces

The i.MX31 and i.MX31L processors each offer a large selection of options for serial device connectivity.

- **I^{2}C**—A two-wire, bidirectional serial bus that provides a simple, efficient method of data exchange, minimizing the interconnection between devices. The i.MX31 and i.MX31L processors each offer three I^{2}C modules.
- **Synchronous Serial Interface or Inter-IC Sound (SSI/I^{2}S) Module**—The i.MX31 and i.MX31L processors offer two SSIs, which are full-duplex serial ports that allow the i.MX31 and i.MX31L processors to communicate with a variety of serial devices. These serial devices can be standard codecs, digital signal processors (DSPs), microprocessors, peripherals, and popular industry audio codecs that implement the inter-IC sound bus standard (I^{2}S) and AC97 standard.
- **Configurable Serial Peripheral Interface (CSPI)**—The i.MX31 and i.MX31L processors each have three CSPIs equipped with data FIFOs. These are master/slave configurable serial peripheral interface modules, capable of interfacing to both SPI master and slave devices.

- **Universal Asynchronous Receiver Transmitter (UART)**—There are five UART modules in each i.MX31 and i.MX31L processor, each capable of providing standard RS-232, non-return-to-zero (NRZ) encoding format, and IrDA-compatible infrared modes.

- **Fast Infra-Red Interface (Fast IR)**—The Fast Infra-Red Interface module is capable of establishing a 0.576 Mbit/sec, 1.152 Mbit/sec, or 4 Mbit/sec half duplex link via an LED and an IR detector. It supports 0.576 Mbit/sec, 1.152 Mbit/sec Medium Infra-Red (MIR) physical layer protocol, and 4 Mbit/sec Fast Infra-Red (FIR) physical layer protocol defined by the IrDA, version 1.4. In addition, the Serial InfraRed (SIR) protocol, which supports data rate 115.2 Kbps or lower, is implemented in the UART modules.

- **1-Wire Interface**—The 1-Wire interface provides the communication line to a 1-Kbit, Add-Only Memory (DS2502), which is used to hold battery characterization information.

- **General Purpose I/O (GPIO)**—The general-purpose input/output peripheral provides dedicated general-purpose pins that can be configured as either inputs or outputs. The GPIO ports support level- or edge-trigger interrupts, and are system-wake-up capable.

  The GPIO has 196 pins total. Most of the I/O signals are multiplexed at SoC level with dedicated functions for pin count efficiency.

2.12 Expansion Ports

The i.MX31 and i.MX31L processors offer five different expansion options for the designer—PCMCIA, SIM, MMC/SD, MS, and ATA Controller. Each expansion port reflects the latest version of the respective specification for that interface. Brief descriptions of each expansion port follow:

- **PCMCIA and Compact Flash**—Each i.MX31 and i.MX31L processors' PCMCIA Host Adapter implements release v2.1 of PCMCIA standard, which defines the use of memory and I/O devices as insertable and exchangeable peripherals for personal computers or PDAs. Examples of these types of devices include Compact Flash, WLAN adapters, and others. The PCMCIA Host Adapter module provides the control logic for PCMCIA socket interfaces and assumes some additional external analog power switching logic and buffering. The additional external buffers allow the host adapter module to support one PCMCIA socket.

- **Subscriber Identification Module (SIM)**—The Subscriber Identification Module interfaces to an external Subscriber Identification Card. It is an asynchronous serial interface adapted for Smart Card communication for e-Commerce applications. The module is compliant with the ISO 7816-3 standard.

- **Multimedia Card/Secure Digital Host (MMC/SD)**—Each i.MX31 and i.MX31L processor implements two MMC/SD slots. The MMC communication is based on an advanced 7-pin serial bus designed to operate in a low-voltage range.

  The Multimedia Card/Secure Digital Host module (MMC/SD) integrates both MMC support along with SD memory and I/O functions. In addition to Multimedia and Secure Digital Cards, the module can be used to communicate to high-bit rate communication devices, such as WLAN 802.11 a/b, Bluetooth wireless technology, and so on.

- **Memory Stick®/Memory Stick Pro® (MS)**—Each i.MX31 and i.MX31L processors' Memory Stick module is a host controller that supports two Memory Stick slots. The MS conforms to

Memory Stick Standard Format Specifications, ver.1.4-00 and *Memory Stick Standard Memory Stick PRO Format Specification,* ver.1.00-01.

- **ATA Controller**—The ATA block of each i.MX31 and i.MX31L processor is an AT attachment host interface and used to interface with IDE hard disk drives and ATAPI optical disk drives. This feature allows designers to attach storage devices at low costs per unit, which is a critical selling point in the portable digital player market. The ATA controller interfaces with ATA devices using the industry standard ATA-6 specification.

2.13 System Control

To ensure optimum power use and clock signal stability, the i.MX31 and i.MX31L processors use the following modules to generate, control, and distribute clock and control signals throughout the i.MX31 and i.MX31L processors and to external devices:

- **Clock Control Module (CCM)**—Provides clock and reset control for each i.MX31 and i.MX31L processor.
- **Digital PLL**—Produces a high-frequency clock signal with a low frequency and phase jitter. The DPLL reference is an external system clock frequency (15 MHz–30 MHz).
- **Frequency Pre-Multiplier (FPM)**—Provides clock generation from a reference clock of a low frequency, for example, a 32 KHz reference clock. The FPM multiplies the reference frequency by a large factor of 640–15360 and produces a high frequency chip clock with a low-frequency jitter. This clock may be used as input to DPLL.
- **I/O Mux Controller (IOMUXC)**—Controls the input and output paths of the I/O Mux, pad properties—for example, pull up/down, hysteresis, and other examples—and interrupt observation.

2.14 Debug

The i.MX31 and i.MX31L processors' debug features are the enablers for hardware and software debug and validation of the silicon, either on an evaluation board, a customer's application board, a closed or opened radio, PDA, or other device. Debugging is used to identify and isolate the cause of failure when running hardware against software in a real-time application.

The i.MX31 and i.MX31L processors' debug hardware also supports system profiling. System profiling is used to improve overall system performance by identifying optimal system configurations.

2.15 Operating Voltage

The operating voltage is as follows:

- I/O voltage: 1.8 V to 3.0 V
- Internal logic voltage: 1.2 to 1.6 V (0.9 V in standby mode), with dynamic and smart control

2.16 Packaging Information

The packaging is as follows:

- Type: 0.5 mm fine pitch MAPBGA

- Dimensions: 14 mm × 14 mm × 1.2 mm
- Balls: 457
- Functional pins: 327 (The remaining balls are for power supplies.)

3   Revision History

Since the release of the previous version of this document, Rev. 0, the document number was changed to MCIMX31PB (from MC1128MX31PB) to reflect a change in the device's generic part number. Also, reference to Enhanced DMA (eDMA) was changed to Smart Direct Memory Access (SDMA) to comply with the terminology of the reference manual.

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