Freescale Semiconductor
Chip Errata

Document Number: MCIMX31CE
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MCIMX31 and MCIMX31L

Silicon Revision: 2L38W and 3L38W, Rev. 1.15 and M45G, Rev. 1.2

This document contains errata information for MCIMX31 and MCIMX31L (i.MX31 and i.MX31L) silicon masks 2L38W and 3L38W, Rev 1.15, and M45G, Rev 1.2. (Errata for Rev 1.0, mask L38W, is excluded as the Rev 1.0 silicon was never made a production part).

Table 1 provides silicon errata information for SoC/system-related issues, the ARM® Platform, and integrated peripherals.

Table 2 provides silicon errata information for the USB Host controller designed by TDI (formerly ARC) partners with ChipIdea.

Third-party errata for the ARM core (ARM Ltd.), Memory Stick® controller (Sony Corp.), MPEG-4 encoder (Hantro), and MBX graphic's accelerator (ARM Ltd. and Imagination Technologies Ltd.) is provided when they exist by their corresponding companies. Refer to Table 3 for details on third-party errata and modules versions used.

1 Errata

Table 1 provides silicon errata information for SoC/system-related issues, the ARM Platform, and integrated peripherals.

Table 1. Chip Errata for i.MX31

Errata ID	Summary	Details	Mask Rev.
MSIls20595	**ModuleAffected:** USB/IO timing **Title:** USB high speed ULPI interface (both Host2 and OTG) does not meet timing in low core voltage **Release Date:** 2/13/2006	**Description:** The path from Clock input to Data output does not meet the required setup timing of output constraints of 6 ns (required by Phillips Transceiver) at 1.2 V. A 1.55-V core voltage (at pin) is required to meet the specified Phillips transceiver timing. **Impact:** USB High Speed requires a core voltage of 1.55 V to meet transceiver timing. Special care must be taken by the OS to ensure high-core voltage at all times when the USB High Speed is used. When the Dynamic Voltage Frequency Scaling (DVFS) feature is used, the DVFS driver must be turned off to prevent the power-management chip from lowering the voltage below the minimal level required. **Workaround:** Core supply voltage must be set to 1.55 V (on pads). **Fix Plan/Status:** Fix Plan: To improve the timing picture, which is currently not guaranteed to work at lowest core voltage, for Rev. 2.0.	2L38W 3L38W M45G
MSIls19340	**ModuleAffected:** Fusebox **Title:** Fusebox access from JTAG (SJC)—different frequency needed for read/write **Release Date:** 2/13/2006	**Description:** When attempting to write-to and read-from the fuse boxes through JTAG, using the same clock period of TCK, the following occurs: When using a clock period lower than 414 ns, the writing process does not execute as expected. This is because the epm_program signal of the fusebox is not stable for a sufficient period of time to be sampled (because of TCK). As a result, thus the epm_ready signal does not have sufficient time to activate (activate low in this case), and as a result of this, the program does not execute. To operate the program correctly, increase the period of TCK; however, when doing so, the reading process does not execute as expected. This is because the ready signal (in the fusebox_analog model) stays low for only 84 ns, so it cannot be captured when the clock period of TCK is very high. Minimal frequency limit for *Read* access is 11.9 MHz. This is due to a short ready signal from the analog part. The maximum frequency limit for write access is 2.4 MHz due to epm_program short assertion time (derived from TCK cycle). **Workaround:** Use different frequency for fuse write and read cycles. **Fix Plan/Status:** Fix planned: To be fixed in Rev. 2.0	2L38W 3L38W M45G
DSPhl23542	**ModuleAffected:** EMI **Title:** Writing in Null Memory locations overwrites the WEIM control registers **Release Date:** 2/13/2006	**Description:** When writing to 0xb802a230 (null memory location), the contents of the WEIM control registers are overwritten. Because of this, it is not possible to access the WEIM CS0, CS1, CS2, CS3, CS4, and CS5 locations. **Fix Plan/Status:** Not Fixed	2L38W 3L38W M45G

Table 1. Chip Errata for i.MX31 (continued)

Errata ID	Summary	Details	Mask Rev.
DSPhl22831	**ModuleAffected:** SDMA **Title:** debug_evt_chn_lines not generated on channel 0 start **Release Date:** 2/13/2006	**Description:** SDMA debug_evt_chn_line[0] is not asserted on channel start event. Operation does function correctly on a restart event. **Workaround:** Switch to another channel and back to restart channel 0 and cause the line to assert. **Fix Plan/Status:** Not Fixed	2L38W 3L38W M45G
DSPhl25117	**ModuleAffected:** RNGA **Title:** Osc_counter_cntrl register will not reset osc1/osc2 if in STOP_CLKS state. **Release Date:** 2/13/2006	**Description:** Writing to the Oscillator Counter Control register will not reset the oscillator counter 1 if the RNGA FSM is in STOP CLOCKS state. The same is true for Counter 2. The problem is caused by the logic to reset the counters, which requires a rising edge of shft_reg_clk_1. This signal is not active during the STOP_CLK state. **Fix Plan/Status:** Not Fixed	2L38W 3L38W M45G
DSPhl22960	**ModuleAffected:** CSPI **Title:** Negation of SS when FIFO empty and SSCTL=0 **Release Date:** 2/13/2006	**Description:** The CSPI negates SS when the FIFO becomes empty with SSCTL= 0. Software cannot guarantee that the FIFO will not drain because of higher priority interrupts and the non-realtime characteristics of the operating system. As a result, the SS will negate before all of the data has been transferred to/from the peripheral. **Fix Plan/Status:** Not Fixed	2L38W 3L38W M45G
TLSbo39790	**ModuleAffected:** CSPI **Title:** Result of writing to CSPI PERIODREG is dependent on internal_ state **Release Date:** 2/13/2006	**Description:** The result of writing to the PERIODREG of the CSPI is dependent on the internal state of the CSPI. The write works only if the CSPI is disabled before changing and then enabled again. **Workaround:** Write to PERIODREG register while CSPI is disabled. **Fix Plan/Status:** Not Fixed	2L38W 3L38W M45G
DSPhl20719	**ModuleAffected:** PWM **Title:** ipp_do_pwmo behavior error when POUTC = 2'b01 **Release Date:** 2/13/2006	**Description:** Currently, ipp_do_pwmo remains 0 for POUTC = 2'b01 and the sample value being used is equal to 0. The correct behavior is that the value of ipp_do_pwmo is equal to 1. **Workaround:** Any waveform that is intended to be generated with POUTC = 2'b01, can be generated with POUTC = 2'b00, setting by suitably alternating sample values. This can be implemented in software. **Fix Plan/Status:** Not Fixed	2L38W 3L38W M45G

Table 1. Chip Errata for i.MX31 (continued)

Errata ID	Summary	Details	Mask Rev.

DSPhl24788	**ModuleAffected:**
	SSI
	Title:
	dma rx requests not generated by SSI after receiver is disabled
	Release Date:
	2/13/2006
		Description:
		Given the scenario:
		1) An external driver is configured to transmit data to SSI2.
		2) After four words are received in Rx FIFO, then rx_en is disabled in SCR register.
		3) DMA is configured to transfer data from Rx FIFO to memory.
		In this situation, the SSI does not generate ipd_ssi_rx1_dmareq_b or ipd_ssi_rx0_dmareq_b. This is because the following logic flaw in ssi_irq.v:
		`assign ipd_ssi_rx1_dmareq_b = !(rx_dma_en & tch_en & rx_en & rx1_dma & ssi_en);`
		`assign ipd_ssi_rx0_dmareq_b = !(rx_dma_en & rx_en & rx0_dma & ssi_en);`
		Notice that rx_en is ANDed in this example logic to generate the requested signals. Therefore, when the receiver (rx_en) is disabled, the DMA Rx request is not generated at all.
		Fix Plan/Status:
		Not Fixed
			2L38W
			3L38W
			M45G

DSPhl20608	**ModuleAffected:** UART **Title:** When the UART is in Doze mode, Xfert of first character transmitted is not completed properly. **Release Date:** 2/13/2006	**Description:** The following test was carried out to pinpoint the errant behavior of the UART: • Set UART Doze bit to 1. Note, in this mode UART must complete any ongoing transmission, and must not begin any new transmission. • Begin transmitting the first character. • Enter into ARM Doze mode. • Continue first character Xfert. • Send second character. • Exit ARM Doze mode. • Transmit third character. • Check Rx FIFO. At the end of this test sequence, the UART Rx FIFO must contain only the first and the third character. UART behavior description: The UART performs this sequence correctly except for the read of the third character. The third character does not input properly into the Rx FIFO. After inspecting the vcd, it was found that the UART does not complete the Xfert of the first character properly. At the end of the Xfert of the first character, the rxd_from_decoder signal is maintained at 0 instead of 1. Because of this erroneous value, the start bit of the third character received is not detected properly, which is why an incorrect character value is read in the Rx FIFO. **Workaround:** No impact on performance. Ensure that the Rx FIFO is empty before entering Doze mode. **Fix Plan/Status:** Not Fixed	2L38W 3L38W M45G

Table 1. Chip Errata for i.MX31 (continued)

Errata ID	Summary	Details	Mask Rev.
DSPhl23796	**ModuleAffected:** UART **Title:** TXD does not mark 1s when transmitter is disabled in the middle of transmission **Release Date:** 2/13/2006	**Description:** In the UART, the TXD/TXD_MUX pin does not begin marking 1s when the transmitter is disabled during the middle of a transmission. This is not consistent with the UART module specifications within the reference manual. In the UART's submodule uart_txblock and its submodule uart_tx_ir, although the signal nrz_encoded becomes 1 two clock cycles after the UART is disabled, it is unable to pass the value to uart_txd_reg because the clock tx_m_clk is no longer available (clock tx_m_clk is gated). **Workaround:** Ensure that TX FIFO is empty before disabling the UART or its transmitter. **Fix Plan/Status:** Not Fixed	2L38W 3L38W M45G
DSPhl22781	**ModuleAffected:** UART **Title:** Transmitting a break condition results in a frame error in the current character transmitting **Release Date:** 2/13/2006	**Description:** For the specified version of IP UART, transmitting a break condition (assert SNDBRK UCR1[4]) results in a frame error in the current character transmission in progress. The reason is the stop bit of current character is destroyed (becomes a narrow pulse other than a valid one). This is not consistent with the UART specification (v1.5 and v1.7). **Fix Plan/Status:** Not Fixed	2L38W 3L38W M45G
DSPhl22423	**ModuleAffected:** UART **Title:** UART does not send one stop bit when configured to send break before TXDC **Release Date:** 2/13/2006	**Description:** In the UART, the send break is enabled during the transmission of the first character. According to the specification, the current character must be transmitted and only then a break should be sent until the send break bit is cleared. This does not happen if breaks are sent after the TXDC bit is set. **Workaround:** Send break only after TXDC bit is set. **Fix Plan/Status:** Not Fixed	2L38W 3L38W M45G
DSPhl19968	**ModuleAffected:** ARM Platform **Title:** AIPS unaligned accesses to 16-bit peripheral **Release Date:** 2/13/2006	**Description:** Unaligned halfword and byte accesses to 16-bit peripherals are not terminated with an error response as stated in the specification, section 4.5. An IP transaction is initiated and incorrect behavior of the IP bus strobes (incorrect strobes assert) may occur. Workaround: Software must not attempt unaligned halfword and byte accesses because these accesses are not supported. **Fix Plan/Status:** Not Fixed	2L38W 3L38W M45G

Table 1. Chip Errata for i.MX31 (continued)

Errata ID	Summary	Details	Mask Rev.
DSPhl19969	**ModuleAffected:** ARM Platform **Title:** AIPS Unaligned (Without Byte Strobes) Accesses to 8-bit Peripheral **Release Date:** 2/13/2006	**Description:** If an unaligned byte accesses (without byte strobes) occurs for 8-bit peripherals a transaction is initiated. The AHB access is not terminated with an error response. It is not clear if the ARM11™ (or any other bus master) can generate this type of access. Workaround: Software must not attempt unaligned byte accesses because these accesses are not supported. **Fix Plan/Status:** Not Fixed	2L38W 3L38W M45G
DSPhl20940	**ModuleAffected:** ARM Platform **Title:** Status Register in ROMPatch **Release Date:** 2/13/2006	**Description:** The status register (ROMPatchSR) in the ROMPatch module always reads zero. The read enable logic is incorrect. **Workaround:** Do not use the ROMPatch Status Register. Use the ETM trace function instead, however, typically this register is not used often. **Fix Plan/Status:** Not Fixed	2L38W 3L38W M45G
DSPhl24192	**ModuleAffected:** ARM Platform **Title:** Non-Word Writes to EVTMON **Release Date:** 2/13/2006	**Description:** Non-word size writes to EVTMON registers can affect the contents of the registers even though they are properly flagged as a bus error. **Workaround:** Only use word writes to the EVTMON registers. **Fix Plan/Status:** Not Fixed	2L38W 3L38W M45G
DSPhl19588	**ModuleAffected:** ARM Platform **Title:** Idle on L2CC **Release Date:** 2/13/2006	**Description:** There is a problem when enabling clock gating in the Level 2 Cache. The IDLE signal becomes active when it should not and the gated clocks can be disabled. This stops the system from functioning until another access occurs on the same port. We can generate the problem by setting up the proper set of pin states and sequences via BFM operation (driving the pins directly without the CPU). It is not clear whether the ARM CPU itself can generate the proper set of pin states and sequences to cause this error. **Workaround:** Do not enable clock gating for the L2CC. The control bit for this is in the clock control module (CLKCTL) and it is reset to force clock gating off. Leave the bit in its reset state to avoid this problem. **Fix Plan/Status:** Not Fixed	2L38W 3L38W M45G

Table 1. Chip Errata for i.MX31 (continued)

Errata ID	Summary	Details	Mask Rev.
DSPhl19594	**ModuleAffected:** ARM Platform **Title:** L2CC Error on All bits of a Burst **Release Date:** 2/13/2006	**Description:** At present, the Level 2 Cache only recognizes errors on the last beat of a burst. Errors on earlier beats are ignored. Note that while this is not ideal, for memory spaces or undefined spaces, entire rows are defined the same way. There will either be all good accesses or all error accesses when a burst occurs. This cannot be assumed for peripheral spaces, but those are typically not cached. **Fix Plan/Status:** Not Fixed	2L38W 3L38W M45G

Table 1. Chip Errata for i.MX31 (continued)

Errata ID	Summary	Details	Mask Rev.

TLSbo65953	**ModuleAffected:**
	ARM Platform
	
	Title:
	FIQ behavior causing aberrant behavior on ARM1136 core when exiting WFI mode
	
	Release Date:
	2/13/2006
		Description:
		The behavior of the FIQ signal to the ARM11 core has been shown to cause a problem when exiting WFI mode. The FIQ signal will toggle after being initially asserted, which is unexpected behavior to the ARM11 core. This particular behavior occurs when core clocks continue to run and, along with particular caching and alignment schemes, can result in a corrupted cache line following a prefetch, and thus unexpected behavior in code. It was also discovered that the core could execute an instruction immediately following the WFI instruction before servicing the FIQ. This errata supersedes and replaces the errata previously reported as TLSbo64855.
		
		Workaround:
		The previous workaround required locating WFI code in a non-cacheable region and including NOPs to “pad” against corruption and pre-execution. This is no longer necessary if the following is implemented; thus, the previous workaround is not recommended.
		The WFI routine should change the clocking mode to 1:1 (ARM:AHB) ratio. After writing to the post-divider register, enough delay must be introduced to ensure that 1:1 mode has been achieved, which can be done by performing a series of “dummy” reads. To determine the delay needed (the number of dummy reads to be performed), one must look at the divide ratios (from HCLK) in the PODFs (post dividers) and then find the LCM (Least Common Multiple) of these to arrive at the worst-case time for the posedges of the clocks to line up. This is required for the CCM to complete the switch to 1:1 mode. After finding the LCM, convert that to IPG cycles based on the IPG divide ratio (generally the IPG bus clock is one-half HCLK). Once the number of IPG cycles have been calculated, add 1 to that number to get the number of reads required to the IP bus (CCM).
		For example, if the CCM HCLK post dividers have divide ratios of 1, 2, and 7, then the LCM is 14 HCLKs. This equals 7 IPG clocks. Thus, 8 reads are required before entering WFI.
		On wakeup, the clocks can then be changed back to the original ratio. This completely prevents the toggle on the interrupt line, and this code can now be located in a cacheable region.
		EXAMPLE:
		mov r0, #0
		ldr r1, =<clock_control_BASE>
		ldr r2, [r1, #OFFSET]
		orr r3, r2, #1TO1MODE
		str r3, [r1, #OFFSET]
		..... // delay while switch to 1:1 occurs
		// In the example stated above, 8 reads are needed
		ldr r3, [r1, #OFFSET] //dummy read 1
		ldr r3, [r1, #OFFSET] //dummy read 2
		...
		ldr r3, [r1, #OFFSET] //dummy read 8
		mcr p15, 0, r0, c7, c0, 4 //WFI
		str r2, [r1, #OFFSET]
		bx lr
		
		Fix Plan/Status:
		Not Fixed
			2L38W
			3L38W
			M45G

Table 1. Chip Errata for i.MX31 (continued)

Errata ID	Summary	Details	Mask Rev.
TLSbo51015	**ModuleAffected:** ATA **Title:** Access to drive register when ATA is in reset state hangs the bus **Release Date:** 2/13/2006	**Description:** When ATA is in reset, reads and writes to the ATA drive registers causes the bus to hang. This has no impact on properly written code. **Workaround:** Not needed—use module properly—that is, never attempt Drive when interface is in reset. **Fix Plan/Status:** Not Fixed	2L38W 3L38W M45G
TLSbo53656	**ModuleAffected:** Integration/Power gating **Title:** Power gating logic leaks during DSM **Release Date:** 2/13/2006	**Description:** Power gates cells are designed such that there is an inverter on the input signal. The input signal may float at MCU power shut-off, causing rush-through current. Therefore**,** when ARM power is cut-off in DSM mode, higher than expected power is drawn because of the floating signals. **Workaround:** Disable power-down mode, which also provides the benefit of saving power. Use SR mode instead. **Fix Plan/Status:** Fix planned: To be fixed in Rev. 2.0	2L38W 3L38W M45G
TLSbo52620	**ModuleAffected:** SSI **Title:** SSI AC97 variable mode bug **Release Date:** 2/13/2006	**Description:** According to AC97 protocol, the AC97 controller (SSI) sends data based on the SLOTREQ bits. When the CODEC sends 0 in SLOTREQ bits, it can mean that the CODEC is requesting data or that a particular channel is powered-down/unimplemented. Within SSI, if SSI receives 0 in SLOTREQ, it means that the CODEC is requesting data; 1 implies that the CODEC does not require data for that slot. Therefore, the SSI has no ability to identify whether the channel is powered down. **Fix Plan/Status:** Not Fixed	2L38W 3L38W M45G
MSIls19391	**ModuleAffected:** CCM/DVFS **Title:** Some DVFS load tracking signals cannot be sampled with div_3_clk **Release Date:** 2/13/2006	**Description:** The load tracking signals of DVFS are intended to stay asserted longer than div_3_clk; however, several signals cannot be used properly for load tracking. **Fix Plan/Status:** Not Fixed	2L38W 3L38W M45G
TLSbo54060	**ModuleAffected:** CCM/DVFS **Title:** DVFS stops working if IPG_CLK freq = HCLK frequency **Release Date:** 2/13/2006	**Description:** When changing IPG_CLK frequency to equal HCLK frequency (IPG postdivider = 1), the DVFS state machine stops working on the next cycle. This is because the switch_to_mpll_finished signal does not get assigned. The mode AHB = IPG clock frequency is not usable in DVFS, and if entered, cannot be exited. **Fix Plan/Status:** Not Fixed	2L38W 3L38W M45G

Table 1. Chip Errata for i.MX31 (continued)

Errata ID	Summary	Details	Mask Rev.
TLSbo54564	**ModuleAffected:** DPTC **Title:** The voltage valid bit (DPVV) in the PMCR0 register in the CCM cannot be updated to DPTC enabling during DPVCR low. **Release Date:** 2/13/2006	**Description:** If bit DPNVCR (PMCR[5]) is not asserted previously, bit DPVV (PMCR[4]) cannot be asserted by the HW (PMIC posedge) as defined by the specification. **Fix Plan/Status:** Not Fixed	2L38W 3L38W M45G
TLSbo54572	**ModuleAffected:** EMI **Title:** Running code that uses SDRAM (16-bit) with data cache off causes the system to hang **Release Date:** 2/13/2006	**Description:** Running Redboot and turning off the data caches causes the system to hang. The RVD or IcePick are unable to communicate to the ARM core. The system must go through reset to recover. This erratum does not apply to DDR. **Workaround:** Programming the SDRAM and SDRAM Controller to Full page mode corrects this behavior. **Fix Plan/Status:** Not Fixed	2L38W 3L38W M45G
TLSbo56802	**ModuleAffected:** IPU **Title:** Interlock condition on MCU access to external GPU on back-to-back single read after single write accesses **Release Date:** 2/13/2006	**Description:** A SW limitation exists for MCU/SDMA access to an external GPU (Graphic Processing Unit) via the IPU slave AHB bus. If the MCU performs a single read from the external GPU via the IPU immediately after a single write, an interlock condition appears. The IPU interface to the GPU works incorrectly in this case. The problem appears when the MCU performs a back-to-back single read after a single write. This occurs when the MCU fetches commands from the cache or the 32-bit DDR. **Workaround:** SW solution—To avoid the interlock, 5 NOPs must be added after a single write before a single read. **Fix Plan/Status:** Fix planned: To be fixed in Rev. 2.0	2L38W 3L38W M45G

Table 1. Chip Errata for i.MX31 (continued)

Errata ID	Summary	Details	Mask Rev.
TLSbo56803	**ModuleAffected:** IPU **Title:** Wrong Y values at frame bottom after deringing in postfilter **Release Date:** 2/13/2006	**Description:** When the IDMAC is heavily loaded and the postfilter performs deringing, some pixels of the last row of the frame may be replicated to the fifth row from the frame bottom edge. Only Y components of the pixels can be replicated. This defect is very rare and is actually invisible on the real video test running on the EVB. The root cause of the defect is that if the IDMAC is heavily loaded, it does not succeed in releasing the postfilter output buffer in time. The postfilter deringing state machine does not check whether the buffer is empty at the last frame row. If deringing is completed before the buffer is released, a Y value of the last row pixel may override the Y value of the pixel located in the fifth row from the frame bottom edge. This is an almost invisible phenomena of pixels replicated on the bottom edge of the screen. **Workaround:** SW must cut the four last lines of the picture to hide this problem. **Fix Plan/Status:** Fix planned: To be fixed in Rev. 2.0	2L38W 3L38W M45G
TLSbo61191	**ModuleAffected:** IPU **Title:** Hanging slave AHB bus for some types of MCU access to the GPU via IPU **Release Date:** 2/13/2006	**Description:** When the MCU directly accesses the external GPU through the IPU, the IPU slave AHB bus hangs in some situations. Specifically, when the MCU generates the BUSY state on the bus during the middle of the access or when performing back-to-back burst accesses. The core might hang if the bus hangs. **Workaround:** Use the IPU DMA channels for transferring data to the external GPU. For writes, the MCU must fill the mirror image in the system memory and enable the IPU DMA channels to transfer the data to the GPU. For reads, the MCU must first enable the DMA channels. On receiving the DMA interrupt, the MCU reads the mirrored data from the system memory. For access to the GPU registers, use the capability of the IPU's low-level access. **Fix Plan/Status:** Fix planned: To be fixed in Rev. 2.0	2L38W 3L38W M45G

Table 1. Chip Errata for i.MX31 (continued)

Errata ID	Summary	Details	Mask Rev.
TLSbo61193	**ModuleAffected:** IPU **Title:** Incorrect SDC combining with local alpha of 0xFF when graphics are in the background **Release Date:** 2/13/2006	**Description:** When graphics are in the background plane and the local alpha mode is used, the SDC incorrectly combines pixels with an alpha value of 0xFF (transparent video). The problem is caused by the wrong control provided by a state machine that controls combining in the SDC. **Workaround:** The workaround is to use key color or global alpha combining options when graphics are in the background plane and alpha is 0xFF. A workaround solution for this application is to simultaneously apply global alpha and color keying modes. The global alpha must be set to 0xFF (transparent video). In screen areas where the graphics must be transparent (visible video), the graphics pixels must be equal to the key color. A standard graphics format can be used (for example RGB565). Because color keying overrides global alpha effects, the graphics will overlay the video in all areas where a graphics color is different from the key color. **Fix Plan/Status:** Fix planned: To be fixed in Rev. 2.0	2L38W 3L38W M45G
TLSbo61195	**ModuleAffected:** IPU **Title:** Cursor gets corrupted before reaching the end of the visible screen buffer. **Release Date:** 2/13/2006	**Description:** The IPU cursor gets corrupted before reaching the end of the visible screen buffer. After that, increasing the column number causes the cursor to cover the entire width of the display. The desired behavior is to be able to move the cursor to the edge of the screen (up to coordinate 240 without any issues.) There are no issues with the cursor blinking or cursor size options. **Workaround:** SW workaround exists. The latest specification includes clarification for correct IPU programming. **Fix Plan/Status:** Not Fixed	2L38W 3L38W M45G
TLSbo61196	**ModuleAffected:** IPU **Title:** As soon as the Foreground window touches the right corner of the screen, it first disappears completely and on the next increase on x coordinate fills up the entire screen. **Release Date:** 2/13/2006	**Description:** When the foreground window touches the right corner of the screen, it first disappears completely and on the next increase the x coordinate fills up the entire screen. This does not happen in the Y direction. In the vertical direction, the window can be moved all the way to the bottom of the screen without any corruption. **Workaround:** SW workaround exists. The latest specification includes clarification for correct IPU programming. **Fix Plan/Status:** Fix planned: To be fixed in Rev. 2.0	2L38W 3L38W M45G

Table 1. Chip Errata for i.MX31 (continued)

Errata ID	Summary	Details	Mask Rev.
TLSbo58425	**ModuleAffected:** FUSEBOX/IO **Title:** FUSE_VDD supply has a short to NVCC2 via ESD diode, causing excessive current when applying high voltage, required for fuse programming **Release Date:** 2/13/2006	**Description:** The FUSE_VDD supply is an analog cell type an_std_lca. This cell has a forward bias diode between the pad where FUSE_VDD is connected and the ovdd, which is NVCC2 (the EMI supply group). Because the EMI supply is 1.8 V, raising the FUSE_VDD to 3 V to program, the e-fuse causes excessive rush-through current via the ESD diode. **Impact:** FUSE_VDD current exceeds the values given in the data sheet, because of the current via the ESD diode. **Workaround:** Increase the NVCC2 supply when performing fuse burning to the maximum allowed by specific DDR memory (~ 1.95 V). Burn at lower allowed FUSE_VDD voltage. **Fix Plan/Status:** Fix planned: To be fixed in Rev. 2.0	2L38W 3L38W M45G
TLSbo59308	**ModuleAffected:** IO/JTAG **Title:** Instability of BSR logic observed at low core voltage **Release Date:** 2/13/2006	**Description:** Instability of BSR logic observed at low core voltage (1.2 V) **Workaround:** Run BSR testing at ~1.6 V only. (1.6 V operation is guaranteed on Tester, by BSDL pattern) **Fix Plan/Status:** Not Fixed	2L38W 3L38W M45G
TLSbo55829	**ModuleAffected:** GPT **Title:** Select of CKIH source to GPT is not possible **Release Date:** 2/13/2006	**Description:** Selection of CKIH source to the GPT is not possible. **Workaround:** None **Fix Plan/Status:** Not Fixed	2L38W 3L38W M45G

Table 1. Chip Errata for i.MX31 (continued)

Errata ID	Summary	Details	Mask Rev.
TLSbo61175	**ModuleAffected:** SIM **Title:** A receiver error when the RCV FIFO is full in the SIM module **Release Date:** 2/13/2006	**Description:** When the SIM module receives continuous data and the RXFIFO is full, the data receive interrupt cannot respond on time. Therefore, the module will cancel the next received data and send a NACK to the card. The card will then re-send the same data if it detects a NACK until the RCVFIFO has a vacant place for this data. In this situation, this data will occasionally be received twice. **Workaround:** Software workaround: 1. Set the value of RDT in RCV_THRESHOLD register as small as possible—that is, to 8, 16, or less. The RCV FIFO full condition occurs with the smaller setting; however, the RCV interrupt is generated more frequently. 2. Set the OEF interrupt enable—the SIM module will set the OEF flag when RCV FIFO is full (overrun). In this interrupt routine, it polls these flags when they receive data. If the OEF flag is equal to 1, it discards the received data and sends the same command, getting the same data again. **Fix Plan/Status:** Fix planned: To be fixed in Rev. 2.0.	2L38W 3L38W M45G
TLSbo60029	**ModuleAffected:** EMI/IO/Power **Title:** Differential mode in DDR causing high current condition at DDR IO pads **Release Date:** 2/13/2006	**Description:** When EMI is programmed to DDR mode, it asserts ddr_input as an input to the DDR IO pads. Because of the use of an improper reference supply, higher than expected IO current is drawn by the DDR IO pads when operating in DDR mode. **Workaround:** None **Fix Plan/Status:** Fixed	2L38W 3L38W

Table 1. Chip Errata for i.MX31 (continued)

Errata ID	Summary	Details	Mask Rev.
TLSbo61213	**ModuleAffected:** CCM/IO/Low Power Modes **Title:** VSTBY signal rises too early, so it cannot be used to shut-off clocks in SR **Release Date:** 2/13/2006	**Description:** VSTBY signal rises too early, so it cannot be used to shut-off clocks in State Retention (SR) mode. VSTBY signal from the CCM module is used to gate the power off when entering SR/DSM modes. When used for cutting-off the CKIH clocks, i.MX31 will not recover from SR state. Because of HW implementation of the CCM, int_holdoff to ARM is not released unless the Lock Ready Flag (mpl_dplrf) is released (when PLL is shut off). Therefore, interrupts to ARM remain blocked in the system and unable to recover from SR mode. CCM requires an additional four CKIH clock cycles between the assertion of VSTBY until CKIH can be shut-off. **Workaround:** *SW workaround:* • Prepare for frequency change, including shut-off AHB masters (IPU, SDMA, RTIC). • When DDR memories are used, SDMA accesses must be complete. • Switch to PLL bypass by clearing the MPE bit in the CCMR register, which turns off the MCU PLL. This changes the core frequency to CKIH. • Enter SR mode. FPM shuts off automatically when entering SR mode. *On Exit from SR:* • Begin with PLL bypass, turn on PLL. Switch to PLL properly; that is, ensure that the DDR frequency changes when working with DDR. **Fix Plan/Status:** Fix planned: To be fixed in Rev. 2.0 with a fix to VSTBY logic to have it asserted last before the core is in LPM modes.	2L38W 3L38W M45G
TLSbo50929	**ModuleAffected:** EMI/DDR, DVFS **Title:** Limited DVFS function in system using DDR memories, such that all points must maintain a fixed AHB frequency **Release Date:** 2/13/2006	**Description:** The DVFS function within a system with DDR memory is limited to the same AHB frequency—that is, the external memory interface frequency is the same across all DVFS voltage and frequency points. A DVFS frequency change between frequency and voltage points is not supported because DDR memory does not allow a frequency change during the middle of a transaction. **Workaround:** Add logic to EMI and CCM to perform a hand-shake for frequency changes similar to entering low-power modes. **Fix Plan/Status:** Not Fixed	2L38W 3L38W M45G

Table 1. Chip Errata for i.MX31 (continued)

Errata ID	Summary	Details	Mask Rev.
TLSbo61214	**ModuleAffected:** SSI **Title:** Defect in I^2S slave mode, causing left/right channel switches **Release Date:** 2/13/2006	**Description:** A defect in I^2S slave mode causes the left and right channels to switch randomly. The SSI begins transmitting and receiving data in I^2S slave mode (async/sync) on the posedge of the frame sync instead of waiting for the negedge of the frame sync when the posedge of the frame sync is encountered first. This scenario occurs when tx_en/rx_en of SSI in the SCR register is disabled in between the frame and enabled after the frame is completed. All other register settings of SSI remain unchanged. **Workaround:** SW Workaround exists. **Fix Plan/Status:** Not Fixed	2L38W 3L38W M45G
TLSbo61142	**ModuleAffected:** CCM/Low Power Mode **Title:** GPIO1_5 pin used as both Power Management IC (PMIC) interrupt and POWERRDY inputs, but must be driven 1 in exit from DSM/SR modes **Release Date:** 2/13/2006	**Description:** Although not explicitly indicated within the specification, GPIO1_5 is a dedicated pad for handshaking with the Power Management IC (PMIC) to exit from State Retention (SR) and Deep Sleep Mode (DSM). CCM input ipp_pmic_int, which is driven by GPIO1_5 pin, must be 1 on exit from SR/DSM modes. This means that the pad must be in its functional mode and not in an alternate GPIO mode. Otherwise, the core will not recover from SR/DSM low-power modes and hang. This is caused by a default value of pmic_int when the non-functional mode is 0. **Workaround:** APP board design and SW must guarantee the following: • GPIO1_5 is in its functional muxing mode when entering LPM mode. • GPIO1_5 is driven to 1 when the core exits LPM mode. **Fix Plan/Status:** Not Fixed	2L38W 3L38W M45G
TLSbo66289	**ModuleAffected:** IPU/Interface timing **Title:** IPU timing parameters IP2, IP3 in Data Sheet (sensor interface) are not covered by Tester program. **Release Date:** 3/15/2006	**Description:** IPU timing IP2, IP3 in sensor interface is not covered for silicon rev 1.15 **Impact:** IPU timing parameters are thus not guaranteed. **Workaround:** **Fix Plan/Status:** Fixed, not yet verified.	2L38W 3L38W

Table 1. Chip Errata for i.MX31 (continued)

Errata ID	Summary	Details	Mask Rev.
TLSbo55792	**ModuleAffected:** SDRAM, DDR, ATA, MSHC. **Title:** Several IO pads lack drive strength or slew rate controls. Specifically critical for SDR signals. **Release Date:** 3/15/2006	**Description:** Weak IO settings without control for SDR/DDR, ATA, and MSHC SDR signals—SDWE, SDBA0, SDBA1, SDCKE0, SDCKE1—have nominal drive by default with no SW control. **Impact:** Board designer have to pay special care to those signals to eliminate timing problems due to over load of the signals. **Fix Plan/Status:** Fixed **Fix Details:** **SDR/DDR Signals** SDBA0—Changed to HIGH drive SDBA1—Changed to HIGH drive SDCKE1—Changed to HIGH drive SDCKE0—Changed to HIGH drive SDWE—Changed to HIGH drive SDQS0—Changed to HIGH drive SDQS1—Changed to HIGH drive SDQS2—Changed to HIGH drive SDQS3—Changed to HIGH drive **Others:** PC_CD1_B—Changed to FAST slew rate PC_CD2_B—Changed to FAST slew rate PC_WAIT_B—Changed to FAST slew rate PC_READY—Changed to FAST slew rate PC_PWRON—Changed to FAST slew rate PC_VS1—Changed to FAST slew rate PC_RST—Changed to FAST slew rate PC_RW_B—Changed to FAST slew rate PC_POE—Changed to FAST slew rate COMPARE—Changed to HIGH drive CAPTURE—Changed to HIGH drive	2L38W 3L38W
TLSbo66305	**ModuleAffected:** DDR/EMI **Title:** Internal DDR IO PAD glitch causing DDR interface delay, and sensitivity at low voltage operation. **Release Date:** 3/15/2006	**Description:** Glitch inside DDR IO pad, on SDQSx signals may lead to glitch on the PAD output, or delay on DDR signals. This is caused when in DDR_input mode, and there is a change in IO direction. **Impact:** EMI-DDR interface timing is not guaranteed to meet specifications. **Fix Plan/Status:** Fixed	2L38W 3L38W

Table 1. Chip Errata for i.MX31 (continued)

Errata ID	Summary	Details	Mask Rev.
TLSbo66295	**ModuleAffected:** MSHC/Interface timings **Title:** MSHC (MemStick) interface timings are not covered for silicon rev 1.15. **Release Date:** 3/15/2006	**Description:** MSHC (MemStick) interface timings are not covered by test program of silicon revision: 1.15. Therefore, the MSHC timings parameter as they appear in the Data Sheet are not guaranteed. **Impact:** MSHC timing parameters are thus not guaranteed. **Fix Plan/Status:** Fixed, not yet verified.	2L38W 3L38W
TLSbo66303	**ModuleAffected:** ETM/Interface timing **Title:** ETM interface timings are not covered for silicon rev 1.15. **Release Date:** 3/15/2006	**Description:** ETM (Embedded Trace Macrocell) interface timings are not covered by test program of silicon revision: 1.15. Therefore, the ETM timings as appear in Data Sheet are not guaranteed. **Impact:** ETM timing parameters are thus not guaranteed. **Workaround:** **Fix Plan/Status:** Fixed, not yet verified.	2L38W 3L38W
TLSbo68334	**ModuleAffected:** Boot/EMI–NFC **Title:** NAND Flash Controller (NFC) fails to correct two single-bit errors if occur on consecutive pages, on data read access. **Release Date:** 4/26/2006	**Description:** In cases when there are single-bit errors in two consecutive page reads, then the error in the second page is not corrected by the NFC. **Impact:** NFC error correction logic is faulty on read accesses and errors in consecutive pages are not fixed. Thus, software must correct the errors in place of the hardware. Special care must be given when booting from a NAND Flash for both 512 bytes, and 2 Kbytes page boot options—see details under Workaround. **Workaround:** In general, when *reading* from NAND Flash, SW must turn off the code correction in HW (ECC) and perform the correction in SW (done by performing error check and correction at the end of each page). When booting from NAND Flash, either external or internal, the NAND Flash Controller (NFC) copies the first 2Kbytes to internal RAM and jumps to beginning of the code. This is done with no option for SW intervention/modification, so the aforementioned general guideline could not be applied. However, due to the nature of this bug, any single-bit error (if found) in the first 512 bytes (first page) is corrected properly, therefore, “special” boot loader code must be placed in those first 512 bytes. The loader code, once executed, must then perform the following: 1. Turn off error correction in HW. 2. Re-load pages 2, 3, and 4 (which comprise the remaining 1.5 Kbytes of code). 3. For every page read, perform error correction in SW. 4. Continue normal execution. **Fix Plan/Status:** Fix planned: To be fixed in Rev 2.0	2L38W 3L38W M45G

Table 1. Chip Errata for i.MX31 (continued)

Errata ID	Summary	Details	Mask Rev.
TLSbo70912	**ModuleAffected:** DDR **Title:** DDR interface faulty when using two chip-select signals. **Release Date:** 06/06/2006	**Description:** When accessing a specific CS (Chip Select) in a “split read access” with wait states, and ckil posedge arrives signaling the controller it is time to refresh, the precharge intended for the inactive chip select alone is given to both chip selects due to faulty $\overline{CS}$ logic. If the next access is a page hit (or the other half of a split access), then the controller will assume the bank is still active and will try to read from the closed bank. **Impact:** The MX31 DDR memory interface cannot work in split read access configuration, and thus, the application board cannot be designed for use of two chip select lines (where each connects to a separate memory IC). **Fix Plan/Status:** Fix planned: To be fixed in Rev. 2.0	2L38W 3L38W M45G
TLSbo72155	**ModuleAffected:** ESDCTL: SDR only **Title:** SDR SDRAM exit self refresh timing is too short for some devices requiring tRC + 1. **Release Date:** 9/7/2006	**Description:** When using external SDR SDRAM with tSREX (also called tXSR, and means self refresh exit to next valid command delay) of more then tRC + 1, the controller may issue auto refresh after exiting manual self refresh too soon, and that may result in errors. The setting of tSREX is not direct, but derived from the tRC value. Relation is as follows: tSREX = (tRC reg value + 1) $\times$ Tcycle (AHB cycle time). In timing, tSREX = tRC + 7.5ns (for 133MHz AHB frequency). tRC (Active to Active timing) if set to higher number than minimal value supported by the memory, will have negligible impact on the performance. This does not affect DDR operation. For DDR, tXSR is hard-wired to 27 clock cycles. At 133 MHz, this yields 7.5ns $\times$ 27 = 202.5ns. **Workaround:** Set tRC to max possible, to meet tSREX timing (Max yields 157.5ns value). This implies tRC = 150ns. Any memories, which support lower tRC value, the impact to performance is negligible. **Fix Plan/Status:** Not Fixed	2L38W 3L38W M45G
TLSbo74193	**ModuleAffected:** EMI: WEIM and NFC **Title:** WEIM and NAND Flash Controller bus sharing may stall if WEIM access starts at the beginning of a NAND Flash Read **Release Date:** 9/7/2006	**Description:** The WEIM and the NAND Flash controller have a special handshake logic that allows them to share the data bus. This logic can stall, prohibiting both of them from using the data bus, if the WEIM access starts at a particular state of the NAND Flash Controller Read State machine. **Workaround:** Do not use WEIM and NAND Flash accesses at the same time. **Fix Plan/Status:** Not Fixed	2L38W 3L38W M45G

Table 1. Chip Errata for i.MX31 (continued)

Errata ID	Summary	Details	Mask Rev.
TLSbo72918	**ModuleAffected:** ESDCTL: SDR **Title:** Cannot use SDR on both chip selects. **Release Date:** 9/7/2006	**Description:** An issue with internal logic causes both CKE0 and CKE1 to go low even though only one chip-select is being accessed. The result is that the SDR SDRAM on the alternate chip-select views CKE as going low which may be mistaken for a power-down operation, therefore the timing for the power-down may not be met (especially as this power-down operation is unintentional). Hence, the chip-selects (CSD0 and CSD1) cannot be used together for SDR memories. This errata does not affect DDR memories. **Workaround:** None. **Fix Plan/Status:** Not Fixed	2L38W 3L38W M45G
TLSbo72912	**ModuleAffected:** Watchdog **Title:** Watchdog (WDOG) timer resets pre-maturely during low power mode. **Release Date:** 9/7/2006	**Description:** After any service sequence of the WDOG Timeout Field (in the Watchdog Control Register, see Reference Manual), it requires two CKIL clocks to reload the WDOG Counter. If the WDZST bit is set (which suspends the WDOG Timer in low power mode) and the system enters low power mode before these two CKIL clocks, the service request is lost. **Workaround:** S/W must ensure that after the WDOG service request, it does not enter low power mode for at least 2 CKIL periods (~61 us). **Fix Plan/Status:** Not Fixed	2L38W 3L38W M45G
TLSbo72605	**ModuleAffected:** WEIM **Title:** WEIM cannot operate with WEIM BCLK equal to AHB clock. **Release Date:** 9/7/2006	**Description:** When enabling the SYNC bit of the WEIM, the burst clock (BCLK) frequency cannot be equal to the AHB (system) clock. This means that for a maximum AHB frequency of 133 MHz, BCLK can be no greater than 66 MHz. **Workaround:** When enabling the synchronous interface of the WEIM, the Burst Clock Divider (BCD) bits must be set to one (divide-by-2) or greater. **Fix Plan/Status:** Not Fixed	2L38W 3L38W M45G
DSPhl26819	**ModuleAffected:** SDHC **Title:** SD1_CMD pin should have pull-up control to eliminate the need for an external resistor. **Release Date:** 9/7/2006	**Description:** The SD1_CMD pin is low by default causing the SD/MMC card to think it has a valid command on wake up. This in turn will cause the card to return a crc error and refuse to boot upon initialization. **Workaround:** Pull up the SD1_CMD line by placing an external 100 K-ohm resistor on this pin. **Fix Plan/Status:** Fix planned: To be fixed in Rev. 2.0	2L38W 3L38W M45G

Table 1. Chip Errata for i.MX31 (continued)

Errata ID	Summary	Details	Mask Rev.
TLSbo71120	**ModuleAffected:** EPIT **Title:** The EPIT Counter may not be updated if the EPITLR is written to multiple times. **Release Date:** 9/7/2006	**Description:** When IOVW = 1 and there are multiple writes of differing values to the EPIT Load Register (EPITLR) within one EPIT counter clock and the last write is 1 ipg_clk before the next rising edge of the counter clock, the last write will not update the EPIT Counter Register (EPITCNT), however, the EPITLR will be loaded with the correct value. This means that the counter will not start counting down from the last value written to the EPITLR. **Workaround:** There are two software work arounds for this bug: 1. Write to the EPITLR with the desired value twice. This ensures that the counter will be updated with the desired value programmed into the EPITLR. 2. For two consecutive (differing) writes to the EPITLR, ensure that the second write is performed at least one counter clock after the first write. **Fix Plan/Status:** Not Fixed	2L38W 3L38W M45G
TLSbo71157	**ModuleAffected:** IIM **Title:** Fusebox Digital Race condition causing the IIM busy status bit to lock. **Release Date:** 9/7/2006	**Description:** A race condition exists in the Fusebox Digital module causing a lock of the IIM busy status bit which prevents further fusing operations unless a reset is performed. **Workaround:** S/W must introduce a delay of at least one CKIL clock cycle (~31 us) between consecutive fuse programming operations. **Fix Plan/Status:** Not Fixed	2L38W 3L38W M45G
TLSbo69244	**ModuleAffected:** NFC **Title:** External boot from NAND Flash not functional when using CKIH as clock source. **Release Date:** 9/7/2006	**Description:** External boot from NAND Flash cannot be used with CKIH as clock source. Because the NFC cannot load the first 2 Kbytes of the NAND Flash fast enough as it only has 8 × CKIL cycles to load the data before the ARM core is brought out of reset. Using CKIL as the clock source, results in a faster clock to the NFC as CKIL is fed through a 1024 frequency pre-multiplier (FPM). This allows the NFC to load the 2 Kbyte data faster and to finish loading the data before the ARM core is brought out of reset. **Workaround:** Use CKIL as the clock source when booting from NAND Flash by setting the external pin CLKSS to low. Software can later override this and switch the CKIH as the clock source after boot by programming the PRCS bits in the CCMR (refer to the Clock Controller Module in the MX31 reference manual). **Fix Plan/Status:** Fix planned: To be fixed in Rev. 2.0	2L38W 3L38W M45G

Table 1. Chip Errata for i.MX31 (continued)

Errata ID	Summary	Details	Mask Rev.
TLSbo67266	**ModuleAffected:** IPU **Title:** R/W signal error for byte enable accesses for asynchronous 68K mode. **Release Date:** 9/7/2006	**Description:** A read/write signal error occurs when the interface type is async sys68k type 1 or type 2 and a read of the upper byte is performed in byte enable mode. When the IPU is setup in this mode, R/W (IPU_WR) should indicate the correct state for both lower and upper byte accesses, however, the observed function is that IPU_WR (R/W) does not indicate correct level for upper byte accesses. No problem occurs for any operations with the sys80 interface, for writing the upper and lower bytes with the sys68k interface, or for reading the full word or the lower byte with the sys68k interface. **Workaround:** There are three possible workarounds for the problem: 1. Use the sys80 interface. No SW limitations are required. 2. If the sys68k interface is used, perform only full 16-bit reads (SW limitation). The desired byte can be extracted from a word by SW. 3. For the sys68k interface, perform ORing of two IPU outputs: DISPB_WR and DISPB_DATA[16]. The OR output should be used as read/write control in sys68k mode with byte enable. This new signal should be used instead of DISPB_WR for this interface. The ORing can be performed on the board or inside the GPU (if possible). The OR function corresponds to the case when the DISPB_WR polarity is 1 for read. No SW limitations are required for this HW workaround. **Fix Plan/Status:** Not Fixed	2L38W 3L38W M45G
TLSbo63646	**ModuleAffected:** PLL, DVFS **Title:** Switch between PLLs for DVFS forces a restart of the target PLL **Release Date:** 9/7/2006	**Description:** When operating DVFS logic and switching between PLLs, (for example, switching from Serial PLL (SPLL) to MCU PLL (MPLL), or from MCU PLL to Serial PLL) the DVFS logic forces a reset to the target PLL when the logic is switched. The impact is as follows: 1. If the target PLL is a source clock to any serial devices, (SSI for instance) then these devices will get a frequency change in the middle of the operation, which will can cause a problem. 2. Switching takes somewhat longer (if no voltage shift is needed), due to the wait for PLL to lock. **Workaround:** None **Fix Plan/Status:** Fix planned: To be fixed in Rev. 2.0	2L38W 3L38W M45G

Table 1. Chip Errata for i.MX31 (continued)

Errata ID	Summary	Details	Mask Rev.
TLSb063573	**ModuleAffected:** SIM **Title:** Glitch on Reset of ICM register in the SIM module. **Release Date:** 9/7/2006	**Description:** The ICM register in the SIM module contains Reset and Set signals. The Set signal connects to system reset and the reset value of the register should be “1”. At the Gate-Level when de-asserting the Set signal, a glitch on the Reset is created, because of the race condition in reset logic. This causes the reset value of the ICM register to be “0” instead of “1” as stated in the specification. **Workaround:** SW Workaround Available: The software should not rely on the reset value of this bit, but instead, write the desired value during initialization. **Fix Plan/Status:** Not Fixed	2L38W 3L38W M45G
TLSbo55829	**ModuleAffected:** GPT **Title:** Missing CKIH source to GPT. **Release Date:** 9/7/2006	**Description:** The CKIH source in not available as a source to the GPT. This means that selecting “011” for the clock source bits in the GPT Control Register is not allowed. **Workaround:** Do not use CKIH (setting of “011” for the clock source select) as source clock for the GPT. **Fix Plan/Status:** Not Fixed	2L38W 3L38W M45G
TLSbo62569	**ModuleAffected:** SDHC **Title:** SDHC timing margin does not meet specifications under different temperature/ voltage conditions. **Release Date:** 9/7/2006	**Description:** Under certain combinations of temperature and voltage, the SDHC will report a command response CRC error and some bits in the response received from the CARD are incorrect.The error bit is never in the same location of the response. As the clock rate is increased, the clock output delay through the pads can cause a data/clock skew issue that results in violating input data setup specs if the input data is latched using a local module clock. This issue is caused by the cumulative delay comprising of the chip internal delay, board delay, card access delay and the clock delay from chip to Card. Under different board designs or different cards, the error window may vary. The fix for this issue is to change the CMD line sample clock from rising edge of the clock to falling edge of the clock. This will provide extra margin of half a cycle. The data signals do not exhibit this issue since they are using the negative edge of the clock to sample the signal. **Workaround:** None. **Fix Plan/Status:** Fix planned: To be fixed in Rev. 2.0	2L38W 3L38W M45G

Table 1. Chip Errata for i.MX31 (continued)

Errata ID	Summary	Details	Mask Rev.
TLSbo78667	**ModuleAffected:** SDHC **Title:** SDHC Multiple-Block Write issues. **Release Date:** 9/7/2006	**Description:** When SDHC transfer multi-block data to Card, it monitors the busy signal (low value of DAT0 driving by CARD) from the card after each block of data is sent to the card. The SDHC waits until the card is ready to send the next block of data. SDHC1 DAT0 is multiplexed with a GPIO and the GPIO signal is polled to determine the card status. However, SDHC2 does not have a GPIO multiplexed with DAT0. **Workaround:** After each multi-block write command (CMD25+CMD12) SW continuously sends CMD13 to read the card status register to determine whether the card busy period is over. This adds overhead to the driver affecting write performance. **Fix Plan/Status:** Not Fixed	2L38W 3L38W M45G
TLSbo81932	**ModuleAffected:** ESD **Title:** MX31 M45G Absolute Maximum Human Body Model (HBM) ESD is 1.5KV. **Release Date:** 10/30/2006	**Description:** M45G mask set does not meet the 2KV Human Body Model (HBM) ESD and was qualified at 1.5KV. Other mask sets meet the 2KV HBM ESD. **Workaround:** None. **Fix Plan/Status:** Fix planned: To be fixed in Rev. 2.0	M45G

Table 1. Chip Errata for i.MX31 (continued)

Errata ID	Summary	Details	Mask Rev.
TLSbo63224	**ModuleAffected:** ESDCTL: DDR **Title:** DDR write timing specs (tDS, tDH) in data sheet not met at low core voltage. **Release Date:** 9/7/2006	**Description:** Timing violations were observed on DDR write timing parameters tDS and tDH (SD17 and SD18 respectively in the data sheet), where a minimum value of 0.95 ns is not met at low core voltages (≤ 1.35 V). **Workaround:** When using DDR, ensure that the core voltage does not fall below 1.35 V to meet the 0.95 ns timing, or choose a DDR memory with less restrictive tDS and tDH timing requirements. **Fix Plan/Status:** Fix planned: To be fixed in Rev. 2.0.	2L38W 3L38W M45G
TLSbo82066	**ModuleAffected:** ARM Platform **Title:** Masking FIQ in the CPU **Release Date:** 11/8/2006	**Description:** The interrupt controller design is such that, whenever FIQ is asserted, the IRQ signal is forced negated. If FIQ is masked inside the CPU (via the CPSR), this can cause the following issues: 1) FIQ can be asserted, but not recognized by the CPU. This forces IRQ to remain negated, so the CPU can never recognize or service the IRQ. 2) IRQ could be asserted, then randomly negated at the moment a masked FIQ is asserted. This could result in unpredictable behavior by the CPU. **Workaround:** Never mask FIQ (inside the CPU via the CPSR) unless IRQ is also masked. If this functionality is needed, FIQ can be masked in the interrupt controller via the FIDIS bit in the INTCNTL register. **Fix Plan/Status:** Not Fixed	2L38W 3L38W M45G

2 USB2 Host Controller Errata

Table 2 lists the errata for the USB host controller by TDI (formerly ARC) partners with ChipIdea.

Table 2. Chip Errata for the USB2 Host Controller of i.MX31

Errata ID	Summary	Details	Mask Rev.
Nashua CR571	**ModuleAffected:** USB2.0 **Title:** Incorrect write enables are used for bytes 2 and 3 write accesses to the ULPI Viewport register **Release Date:** 2/13/2006	**Description:** The incorrect write enables are used for bytes 2 and 3 write accesses to the ULPI Viewport register. This problem does not occur with 32 bit accesses. **Fix Plan/Status:** Not Fixed	2L38W 3L38W M45G
Nashua CR574	**ModuleAffected:** USB2.0 **Title:** When device disconnects in full-speed, the xcvr_select transitions through HS **Release Date:** 2/13/2006	**Description:** In Host mode when the device disconnects during full speed, the xcvr_select transitions through high speed. **Fix Plan/Status:** Not Fixed	2L38W 3L38W M45G
Nashua CR583 3U	**ModuleAffected:** USB2.0 **Title:** Data pulsing lasts for 8 ms when SRP is enabled regardless of the state of the bus **Release Date:** 2/13/2006	**Description:** When the SRP accelerator is enabled, data pulsing lasts for 8 ms regardless of the state of the bus, as opposed to ceasing when the core detects that a_vbus_vld is asserted. **Fix Plan/Status:** Not Fixed	2L38W 3L38W M45G
Nashua CR584	**ModuleAffected:** USB2.0 **Title:** Host missing interrupt on a resume after suspend **Release Date:** 2/13/2006	**Description:** The host does not detect an interrupt on a resume after suspend, and the port-change-control interrupt does not go active, and no port-change-toggle occurs. **Workaround:** Software: Monitor the SOFs. If SOFs are generated then the port is resumed. **Fix Plan/Status:** Not Fixed	2L38W 3L38W M45G

Table 2. Chip Errata for the USB2 Host Controller of i.MX31 (continued)

Errata ID	Summary	Details	Mask Rev.
Nashua CR585	**ModuleAffected:** USB2.0 **Title:** Disconnect bit is not visible, when host is running in Test_Force_Enable mode **Release Date:** 2/13/2006	**Description:** When host is running in Test_Force_Enable mode, the disconnect bit is not visible. **Fix Plan/Status:** Not Fixed	2L38W 3L38W M45G
Nashua CR591	**ModuleAffected:** USB2.0 **Title:** Core sends packet traffic (SOF's) when in TEST_MODE_SE0 **Release Date:** 2/13/2006	**Description:** The host UTMI+ core sends packet traffic (SOF's) when in TEST_MODE_SE0. **Fix Plan/Status:** Not Fixed	2L38W 3L38W M45G
Nashua CR609	**ModuleAffected:** USB2.0 **Title:** The host core sends an extra byte of data after the Keep Alive for directly attached low speed devices **Release Date:** 2/13/2006	**Description:** The host core sends an extra byte of data after the Keep Alive for directly attached low speed devices. **Impact:** Does not cause any interoperability problems. **Fix Plan/Status:** Not Fixed	2L38W 3L38W M45G
Nashua CR590	**ModuleAffected:** USB2.0 **Title:** The ULPI TX state machine locks-up if the peripheral disconnects immediately prior to a packet transmit **Release Date:** 2/13/2006	**Description:** Host, FS/LS Only: The ULPI TX state machine lock-ups when the peripheral disconnects immediately prior to a packet transmit. The ULPI sends an RXCMD to indicate that there is an SE0 on line state instead of an ACK as the target did not respond. The core must wait 2.5 ms to ensure that this is really a disconnect before recognizing it as such. Meanwhile, the transmit state machine re-tries the previous transaction—that is, the combination of the events where the SE0 was registered and the first transition on the bus caused an erroneous EOP to be detected and the transmit state machine locked up. The core issues the port change detect interrupt which shows that a disconnect has occurred, however, there is no indication that the ULPI transmit state machine is locked up. **Impact:** Critical, must use SW workaround. **Workaround:** Software: Reset the core in SPH and OTG after an FS peripheral disconnect, in an MPH wait until the transfers on all other ports has completed, then reset the core. **Fix Plan/Status:** Not Fixed	2L38W 3L38W M45G

Table 2. Chip Errata for the USB2 Host Controller of i.MX31 (continued)

Errata ID	Summary	Details	Mask Rev.
Nashua CR597	**ModuleAffected:** USB2.0 **Title:** A pre-empted tx packet causes the ulpi_tx state-machine to lock-up **Release Date:** 2/13/2006	**Description:** A pre-empted tx packet causes the ulpi_tx state machine to lock-up. In this context tx means that the process of putting the data out onto the bus is in progress, not that a packet is queued for later transmission. If working as host, the USB will not begin transmitting the next packet until the results of the previously received packet are known. It is possible, however, that a malfunctioning device is transmitting. If working as a device, the USB will only begin to transmit in response to a receive packet (a host must never send another packet in the interpacket interval). This anomaly only shows up in testing because the link is taken out of test packet mode without resetting the core as required by the USB2.0 specification. **Fix Plan/Status:** Not Fixed	2L38W 3L38W M45G
Nashua CR610	**ModuleAffected:** USB2.0 **Title:** Previous LS_THRU_HUB packet causes next FS packet to be sent as LS_THRU_HUB **Release Date:** 2/13/2006	**Description:** Previous LS_THRU_HUB packet causes the next FS packet to be sent as LS_THRU_HUB. **Fix Plan/Status:** Not Fixed	2L38W 3L38W M45G
Nashua CR566	**ModuleAffected:** USB2.0 **Title:** Missing reset on register iface_ser_sel_r in the ULPI block. **Release Date:** 2/13/2006	**Description:** Missing reset on register iface_ser_sel_r in the ULPI block. This errata was released in the 4.1.2 version of the ULPI product. **Fix Plan/Status:** Not Fixed	2L38W 3L38W M45G
Nashua CR570	**ModuleAffected:** USB2.0 **Title:** ULPI logic generates a register write request without register access to j or k traffic when the test mode is set to either test_j or test_k **Release Date:** 2/13/2006	**Description:** Setting the test mode to either test_j or test_k causes the ULPI logic to generate a register write request (to disable bit stuffing) and to generate either the j or k traffic. However, there is a register in the logic path for the register access request and not one for the j/k traffic. This anomaly causes the j or k access to the ULPI port and lock-out the register write. **Fix Plan/Status:** Not Fixed	2L38W 3L38W M45G

Table 2. Chip Errata for the USB2 Host Controller of i.MX31 (continued)

Errata ID	Summary	Details	Mask Rev.
Nashua CR572	**ModuleAffected:** USB2.0 **Title:** ULPI—set/clear on IFACE and OTG registers always clears bits that are controlled by SW **Release Date:** 2/13/2006	**Description:** ULPI—set/clear on IFACE and OTG registers always clears bits that are controlled by SW. The values for the registers clear access for these bits are inverted. The HW will clear any bit set by SW when an autonomous HW register access is executed. **Fix Plan/Status:** Not Fixed	2L38W 3L38W M45G
Nashua CR577	**ModuleAffected:** USB2.0 **Title:** Count of inter-packet gap differs from the ULPI specification **Release Date:** 2/13/2006	**Description:** The ULPI specification allows between 15–24 clocks for Host Transmit to Transmit inter-packet gap, however this time starts with the assertion of stp in HS, in full speed the time starts from the receipt of the RX CMD packet that indicates SE0-J transition. The ULPI code begins timing from the FS condition instead of the assertion of STP. **Fix Plan/Status:** Not Fixed	2L38W 3L38W M45G
Nashua CR579	**ModuleAffected:** USB2.0 **Title:** ULPI interface does not detect the end of a receive packet on the deassertion of dir only **Release Date:** 2/13/2006	**Description:** The ULPI interface does not detect the end of a receive packet on the deassertion of dir only. **Fix Plan/Status:** Not Fixed	2L38W 3L38W M45G

Table 2. Chip Errata for the USB2 Host Controller of i.MX31 (continued)

Errata ID	Summary	Details	Mask Rev.
ARC DDTS not available 17U	**ModuleAffected:** USB2.0 **Title:** Transmit state machine locks up when FS port is disconnected during back-to-back transmission **Release Date:** 2/13/2006	**Description:** When an FS port is disconnected during back-to-back transmit transactions—for example, OUT token followed by DATA—the transmit state machine can lock up, depending on precisely when the port was disconnected. The only recovery option is a hard or soft reset of the USB block. This bug effects FS, ULPI, host only operation. **Workaround:** There are some possible software workarounds. These involve issuing a soft reset when a Disconnect event occurs. The reset can be further qualified to only be issued when ULPI mode is operating at FS. This should work fine for OTG, SPH and the MPH when only one port is active. However, when multiple ports of the MPH are active, then the reset can cause data to be lost on the ports that remain connected. This is because the soft reset is not port independent. So, if there is activity on the other port, the reset will cause the data on that port to be lost. To prevent this, the software can possibly, wait for or create, a window of inactivity to reset the controller. **Fix Plan/Status:** Not Fixed	2L38W 3L38W M45G
Nashua CR579	**ModuleAffected:** USB2.0 **Title:** A remote wakeup can be interpreted as a disconnect in ULPI mode of USBOTG **Release Date:** 2/13/2006	**Description:** A remote wakeup could be interpreted as a disconnect in ULPI mode of USBOTG. This issue involves the latency in asserting synchronous mode. In some instances, the host does not properly latch the K state. The core then determines that it woke-up in a J state. Eventually the host does not takeover the resume, and will later interpret an SE0 and presume a disconnect occurred. The latency in asserting synchronous mode is fixed, so this is no longer an issue. **Fix Plan/Status:** Not Fixed	2L38W 3L38W M45G

3 Embedded Third Party Module Errata

The i.MX31 uses embedded third party modules for which there are separate errata documentation as relevant. This information is provided in the Table 3.

Table 3. Third Party Errata

Module Name	Third Party Source	Module Version (used by i.MX31)	Errata Source
MSHC (Memory Stick Host Controller)	Sony Corp.	1.3	No Known Errata
USB (Universal Serial Bus Controller)	TDI	4.0.2 [1]	See Table 2
MBX (Graphics Accelerator, aka GPU)	ARM Ltd.	Lite 1_2_0	MBX ERRATA 1.0.155a External Issue MBXLITE1_2_0. 30Mar2005
MPEG-4 Encoder	Hantro	1_3	No Known Errata
ARM11™ Core	ARM Ltd.	ARM1136JF-S™ r0p2 (mask L38W), and r0p4 (mask 2L38W)	ARM1136J-S/ARM1136JF-S (AT310/AT260) Rev. 10.0, 27Jan2005
L2 Cache Controller	ARM Ltd.	ARM1136JF-S r0p2_01 (L38W), r0p2_02 (2L38W)	ARML210 Errata List AS006-PRDC-003350 6.1

[1] This includes the critical bug fix that relates to ULPI High Speed support (Ver. 4.2), as follows:

[Host/OTG/Multi-Host; ULPI Only] The ULPI logic was not properly decoding RxActive when it was encoded in its immediate form (**dir** and **nxt** simultaneously asserted with **dir** previously low). If there was no intervening RxCMD to indicate RxActive before the receive data, the link will fail the next receive packets as if a BTO had occurred while waiting for the data phase of the transfer. (Nashua CR569)

4 Revision History

Table 4 lists the document changes.

Table 4. Revision History

Date	Sections Affected	Change(s)
11/2006	Section 1, “Errata”	• Added errata: TLSbo81932, TLSbo63224, TLSbo82066 • Modified errata TLSbo65953 to include more details on the workaround. • Modified errata TLSbo61175 to say “Fix planned: To be fixed in Rev. 2.0.”

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