MCIMX31 and MCIMX31L Applications Processors Reference Manual

Addendum

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About This Book

This addendum supplements—and should be used in conjunction with—the MCIMX31 and MCIMX31L Applications Processors Reference Manual, Rev. 2.2 (document number MCIMX31RM). The content of this addendum completely replaces Chapter 4, “Signal Descriptions and Pin Assignments,” and Chapter 13, “IC Identification (IIM),” in MCIMX31RM Rev. 2.2.

Audience

This addendum is intended for users of the MCIMX31 and MCIMX31L Applications Processors Reference Manual, Rev. 2.2.

Revision History

The following table summarizes revisions to this document since the previous release (Rev. 1).

Revision History

Location	Revision
Chapter 4, “Signal Descriptions and Pin Assignments”	In Rev. 2 of this addendum there has been a significant reorganization of the entire chapter. The block diagrams have been simplified and the overview and initial module description has been expanded. A new section (**ATA Routing Options**) has been added to assist the customer in understanding the complex ATA configuration schemes.
Chapter 13, “IC Identification (IIM)”	In Rev 1 of this addendum the values of the Silicon Revision (SREV) register were changed to accurately reflect the silicon ID values for all of the current builds of MCIMX31 and MCIMX31L. No changes have been made to this chapter in Rev 2.
Chapter 19, “Enhanced SDRAM Controller (ESDCTL)” ”	The value of one cell in table 19-2 **SDRAM (SDR and LPDDR) Command Encoding** table was changed from X to H to ensure compliance with the naming conventions of the JEDEC specification. Nothing else in the chapter has changed nor has any setting in the silicon changed. The changed value is indicated in red.

Chapter 4
Signal Multiplexing

This chapter identifies and describes the I/O module that configures and controls the multiplexing of signals going from and to the i.MX31 and i.MX31L. It also provides information about the I/O needed to configure and operate this module.

NOTE

In previous versions of the i.MX31 reference manual this chapter was named “Signal Descriptions and Pin Assignments”. The title was changed to Signal Multiplexing to be consistent with other documentation within this family of ICs.

4.1 Overview

This section provides an overview of the configuration and operation of the I/O Mux Controller (IOMUXC) module. The IOMUXC module shown in Figure 4-1 is composed of three hardware blocks:

- **MUX**—Routes signals to and from the I/O
- **Buffers**—Logic level converters and drivers for interfacing the signals to the external contacts of the IC. I/O characteristics of each line are determined by these buffers.
- **Control Registers**
  - Software Mux Control (SW_MUX_CTL)—These register control the configuration of the signal lines connecting the On-chip peripherals to the contacts. See SW_MUX_CTL registers.
  - I/O Line Characteristics (SW_PAD_CTL)—These registers configure features such as pull-ups, drive strength, and hysteresis. See SW_PAD_CTL registers.

While there is interaction between the GPIO and the IOMUXC, the operation of the GPIO is described in Chapter 5, “General Purpose Input/Output (GPIO).”

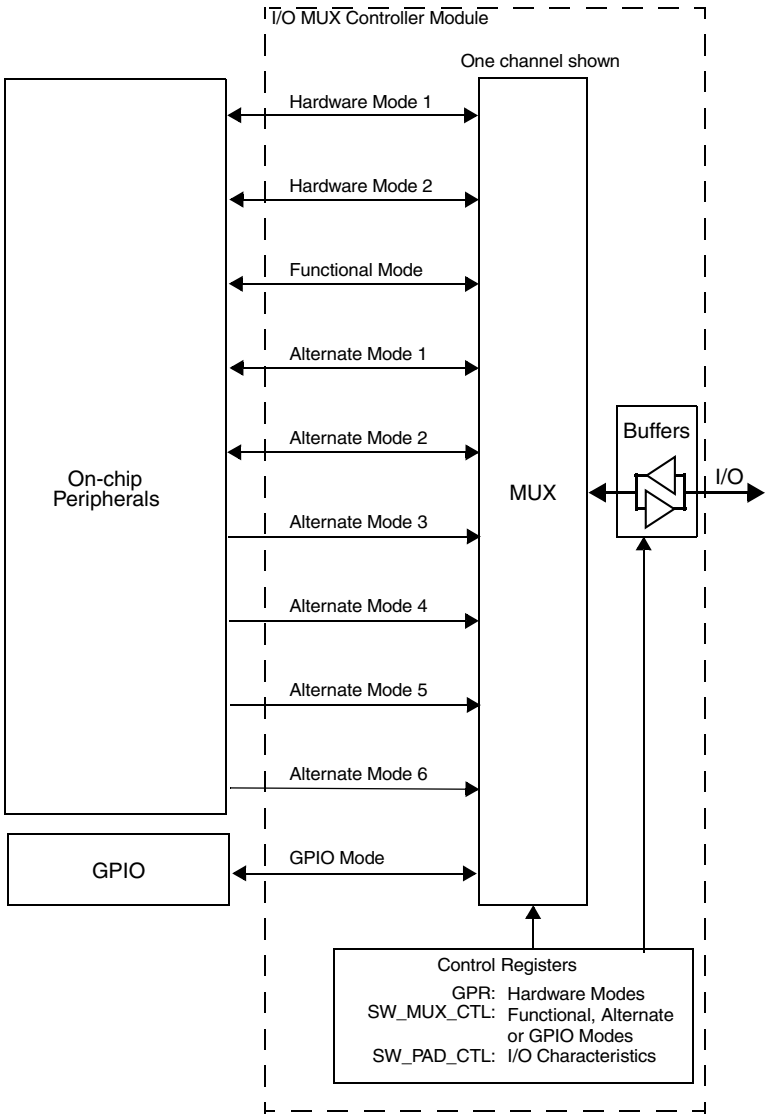

Figure 4-1. I/O Signal Multiplexing Block Diagram

4.2 IOMUX Controller (IOMUXC)

The IOMUXC registers control features in the IOMUXC. These registers perform the following tasks:

- Controls the IOMUX input and output paths.
- Controls I/O line properties such as pull-up, pull-down, and hysteresis.
- Monitors off-chip interrupts.

Figure 4-2 shows the registers that control the IOMUXC.

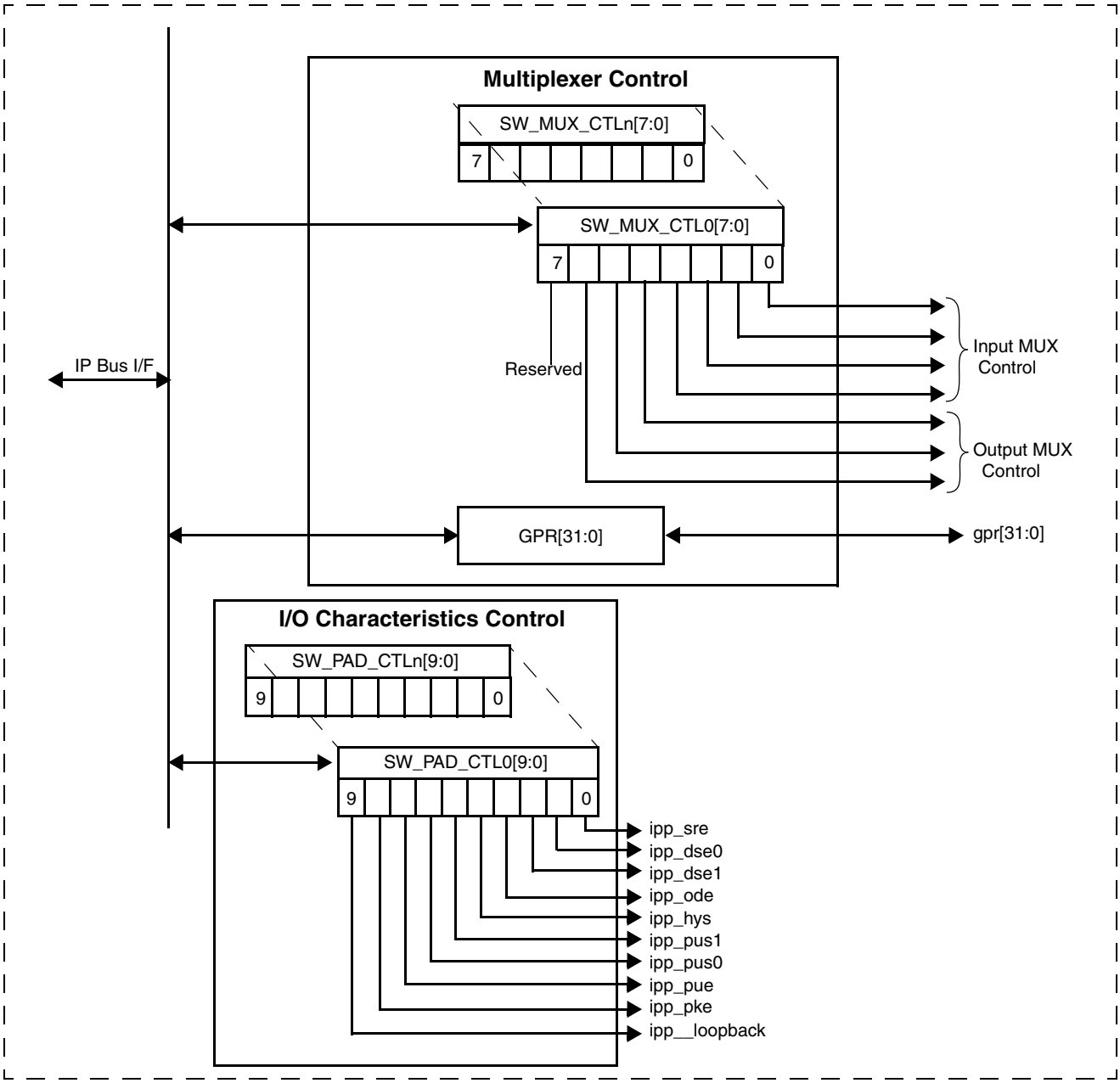

Figure 4-2. IOMUXC Registers

4.2.1 Software Multiplexor Control (SW_MUX_CTL)

The SW_MUX_CTL block consists of registers that control each IOMUX on an individual I/O line basis. The SW_MUX_CTL registers are partitioned into 4×8 bit fields. Each field is mapped to a specific I/O line and is partitioned as follows: four bits to control the input path, three bits to control the output path, and one reserved bit.

4.2.2 Software Pad Control (SW_PAD_CTL)

The SW_PAD_CTL block consists of registers that control the characteristics of each I/O line. The SW_PAD_CTL registers are partitioned into 3×9 bit fields, with each field mapped to a specific I/O line. Each field in the register controls several parameters of the I/O characteristics (for example, pull-up/pull-down, keeper, max drive, hysteresis, and open-drain).

4.3 Memory Map and Register Definition

Table 4-1 shows the IOMUXC memory map.

Table 4-1. IOMUX Memory Map

Address	Register	Access	Reset Value	Section/Page
0x43FA_C008	General Purpose Register (GPR)	R/W	0x0000_0000	4.3.2/4-5
0x43FA_C00C to 0x43FA_C150	Software MUX Control Register (SW_MUX_CTL)	R/W	See register descriptions.	4.3.3/4-9
0x43FA_C154 to 0x43FA_C308	Software Pad Control Register (SW_PAD_CTL)	R/W	See register descriptions.	4.3.7/4-77

4.3.1 Register Summary

Figure 4-3 shows the key to the register fields and Table 4-2 shows the register figure conventions.

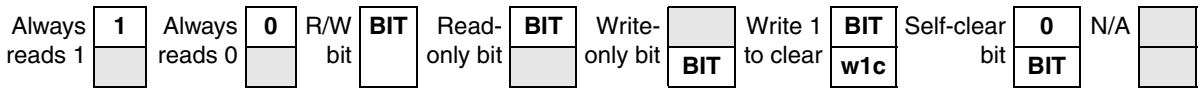

Figure 4-3. Key to Register Fields

Table 4-2. Register Figure Conventions

Convention	Description
	Depending on its placement in the read or write row, indicates that the bit is not readable or not writable.
FIELDNAME	Identifies the field. Its presence in the read or write row indicates that it can be read or written.
Register Field Types	
r	Read only. Writing this bit has no effect.
w	Write only.
rw	Standard read/write bit. Only software can change the bit's value (other than a hardware reset).
rwm	A read/write bit that may be modified by a hardware in some fashion other than by a reset.
w1c	Write one to clear. A status bit that can be read, and is cleared by writing a one.
Self-clearing bit	Writing a one has some effect on the module, but it always reads as zero.
Reset Values	

Table 4-2. Register Figure Conventions (continued)

Convention	Description
0	Resets to zero.
1	Resets to one.
—	Undefined at reset.
u	Unaffected by reset.
[*signal_name*]	Reset value is determined by polarity of indicated signal.

Table 4-3. IOMUXC Register Summary

Field		31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
		15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0x43FA_C008	R	GPR[31:0]															
	W																
	R																
	W																
0x43FA_C00C to 0x43FA_C150	R	SW_MUX_CTLx[31:0]															
	W																
	R																
	W																
0x43FA_C154 to 0x43FA_C308	R	SW_PAD_CTLx[31:0]															
	W																
	R																
	W																

4.3.2 General Purpose Register (GPR)

The General Purpose Register (GPR) is used to configure the IOMUXC. Bits in the GPR control combinations of predefined I/O type signals in the IOMUXC which are prioritized as Hardware modes 1 and 2 (HW1 and HW2). The priority of these hardware modes is shown in Table 4-7. Figure 4-4 shows the GPR register; Table 4-4 provides its field descriptions, and the bit definitions. Each bit controls a combination of I/O lines, functions or modes. The operation of each bit is defined in Table 4-5.

0x43FA_C008 Access: User Read/Write

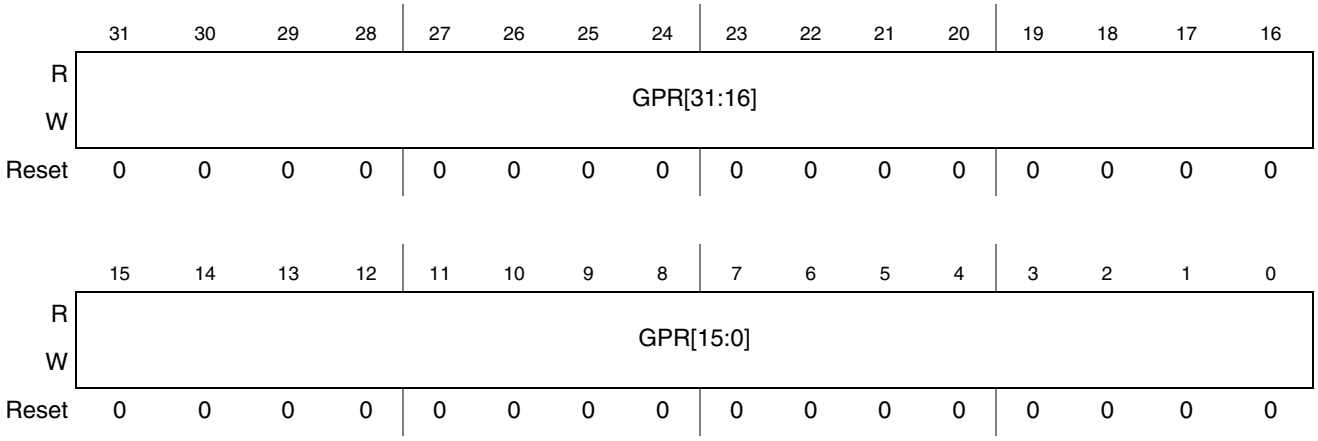

Figure 4-4. General Purpose Register (GPR)

Table 4-4. GPR Register Field Description

Name	Description
31–0 GPR[31:0]	Each bit in this register controls a combination of I/O Type signals or selection/modes. The signals are routed through the IOMUXC, providing 32 combinations of settings.

Table 4-5 shows which signals or hardware modes are controlled by each GPR bit. The multiplexing data about the signals being controlled is listed in Table 4-8 on page 40.

Table 4-5. Hardware Mode Definitions by GPR Bit Position

Bit	Definition	HW Mode	GPR bit = 0	GPR bit = 1
GPR[0]	Selects FIR or UART2 SDMA events	—	UART2 DMA requests are selected for DMA events 16 and 17.	FIR DMA requests are selected for DMA events 16 and 17.
GPR[1]	Forces all DDR type contacts to DDR Drive Strength setting.	—	Inactive (recommended)	Forces DDR type I/O contacts to DDR mode[1]
GPR[2]	Overrides the Full UART group default signals on page 4-62 with CSPI1	HW1	Inactive	Replaces Full UART Group with CSPI1 signals.
GPR[3]	Overrides the PWMO default signal with the ATA IORDY signal	HW1	Inactive	Enable ATA IORDY signal on PWMO contact.
GPR[4]	Overrides the USBH2 default signals with the following ATA signals • DA[2:0] • DMARQ • BUFFER_EN • INTRQ	HW1	Inactive	Enable ATA signals on USBH2 contacts
GPR[5]	Overrides the EMI Group NANDF default signals with ATA Data[13:7]	HW1	Inactive	Enable ATA DATA7-13 on NANDF contacts.

Table 4-5. Hardware Mode Definitions by GPR Bit Position (continued)

Bit	Definition	HW Mode	GPR bit = 0	GPR bit = 1
GPR[6]	Overrides the default EMI Group signals with the following ATA signals: • DA[2:0] • DMARQ • BUFFER_EN • INTRQ	HW2	Inactive	Enable ATA signals on NANDF contacts
GPR[7]	Override the default IPU (CSI) /I2C Group signals with the ATA Data.	HW1	Inactive	Enable DATA0-13 signals of ATA on IPU (CSI) and DATA14-15 on I2C
GPR[8]	Overrides the default AudioPort 3 and AudioPort6 Group signals with the ATA Data signals.	HW1	Inactive	Enable DATA7-10 signals of ATA on AudioPort3 and DATA11-13 on AudioPort6
GPR[9]	Overrides the default Timer/CSPI1 Group signals with ATA Data signals.	HW1	Inactive	Enable ATA DATA14-15 on Timer Group contacts and DATA0-6 on CSPI1 Group contacts.
GPR[10]	Overrides the default CSPI1 signals with the following ATA signals • DA[2:0] • DMARQ • BUFFER_EN • INTRQ	HW2	Inactive	Enable ATA signals on CSPI1 Group contacts
GPR[11]	Overrides the default AudioPort 3 and AudioPort6 Group signals with USBH2 signals.	HW2	Inactive	Enable USBH2 signals on AudioPort 3 and AudioPort6
GPR[12]	Selects either CSD0 or WEIM on EMI CS2 contact.	—	CSD0 is selected for EMI CS2	WEIM is selected for EMI CS2
GPR[13]	Selects either CSD1 or WEIM on EMI CS3 contact.	—	CSD1 is selected for EMI CS3	WEIM is selected for EMI CS3
GPR[14]	Selects either CSPI1 or UART3 DMA requests.	—	CSPI1 DMA request is selected for events 8 and 9.	UART3 DMA request is selected for events 8 and 9.
GPR[15]	Selects either External or MBX DMA requests.	—	External DMA Request2 is selected for event 14	MBX DMA request is selected for event 14.
GPR[16]	Enables Tamper Detect Logic.	—	Inactive	Tamper detect logic is enabled.
GPR[17]	Overrides default DSR_DCE1 signal with the USBOTG_DATA4 signal.	HW2	Inactive	Enable USBOTG_DATA4 on DSR_DCE1 contact.
GPR[18]	Overrides the default Full UART Group signals DCD_DCE1, DSR_DCE1 and RI_DCE1 with USBOTG_DATA[5:3].	HW2	Inactive	Enable USBOTG_DATA[5:3] on Full UART Group contacts

Table 4-5. Hardware Mode Definitions by GPR Bit Position (continued)

Bit	Definition	HW Mode	GPR bit = 0	GPR bit = 1
GPR[19]	Selects either SDHC1 or MSHC1 DMA requests.	—	SDHC1 DMA Request Is Selected for event 20	MSHC1 DMA request is selected for event 20.
GPR[20]	Selects either SDHC2 or MSHC2 DMA requests.	—	SDHC2 DMA Request Is Selected for event 21	MSHC2 DMA request is selected for event 21.
GPR[21]	Selects GPIO3_0 or SPLL_BYPASS_CLK. **Note:** SPLL_BYPASS_CLK is intended for testing purposes.	HW1	Inactive	Enable SPLL clock bypass through GPIO3_0 contact.
GPR[22]	Selects GPIO3_1 or UPLL_BYPASS_CLK. **Note:** UPLL_BYPASS_CLK is intended for manufacturing testing.	HW1	Inactive	Enable UPLL clock bypass through GPIO3_1 contact.
GPR[23]	When MSHC2 clock is selected using Alternate Mode 2, this bit controls the drive strength on PC_CD1_B as either a standard/high or maximum drive strength.	—	Standard or high drive strength	Maximum drive strength
GPR[24]	When MSHC2 clock is selected using Alternate Mode 2, this bit controls the output on PC_CD1_B as either a slow or fast slew rate signal	—	Slow slew rate	Fast slew rate
GPR[25]	Selects either CSPI3 or UART5 DMA requests.	—	CSPI3 DMA requests are selected for events 10 and 11.	UART5 DMA requests are selected for events 10 and 11.
GPR[26]	Overrides the default Keypad Group signals with the following ATA signals • DA[2:0] • DMARQ • BUFFER_EN • INTRQ	HW1	Inactive	Enable ATA signals on Keypad Group contacts
GPR[27]	Overrides the default signal SFS6 with USBH1_SUSPEND.	HW1	Inactive	Enable USBH1_SUSPEND signal on SFS6 contact.
GPR[28]	Enables USBOTG loopback **Note:** This is intended for manufacturing testing.	—	Inactive	Turn on sw_input_on (loopback) on some USBOTG contacts
GPR[29]	Enables USBH1 loopback **Note:** This is intended for manufacturing testing.	—	Inactive	Turn on sw_input_on (loopback) on some USBH1 contacts
GPR[30]	Enables USBH2 loopback **Note:** This is intended for manufacturing testing.	—	Inactive	Turn on sw_input_on (loopback) on some USBH2 contacts
GPR[31]	Enables DDR Drive Strength setting on the CLKO contact.	—	Inactive	Enable DDR mode on CLKO contact

[1] Setting this bit is not recommended as it may produce excessive overshoot.

4.3.3 Software Multiplexor Control Register (SW_MUX_CTL)

The SW_MUX_CTL register controls the IOMUX. Figure 4-5 describes an example generic SW_MUX_CTL register. Table 4-6 provides the register's field descriptions; Table 4-7 lists its priorities.

0x43FA_C00C
to
0x43FA_C150

Access: User Read/Write

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R		SW_MUX_CTL_SIGNAL 4								SW_MUX_CTL_SIGNAL 3						
W		SW_MUX_OUT_EN			MUX2_IN	MUX1_IN	FUNC_IN	GPIO_PSR/ISR		SW_MUX_OUT_EN			MUX2_IN	MUX1_IN	FUNC_IN	GPIO_PSR/ISR
Field Bits	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R		SW_MUX_CTL_SIGNAL 2								SW_MUX_CTL_SIGNAL 1						
W		SW_MUX_OUT_EN			MUX2_IN	MUX1_IN	FUNC_IN	GPIO_PSR/ISR		SW_MUX_OUT_EN			MUX2_IN	MUX1_IN	FUNC_IN	GPIO_PSR/ISR
Field Bits	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0

Figure 4-5. SW_MUX_CTL Register

Table 4-6. SW_MUX_CTL Register Field Descriptions

Register Bit	Bit Name	Setting
SW_MUX_CTL[31] SW_MUX_CTL[23] SW_MUX_CTL[15] SW_MUX_CTL[7]	—	Reserved

Table 4-6. SW_MUX_CTL Register Field Descriptions (continued)

Register Bit	Bit Name	Setting
SW_MUX_CTL[30:28] SW_MUX_CTL[22:20] SW_MUX_CTL[14:12] SW_MUX_CTL[6:4]	sw_mux_out_en	**MUX Output Selection** 000 GPIO DR (data register) output 001 Functional output 010 Alternate mode 1 output 011 Alternate mode 2 output 100 Alternate mode 3 output 101 Alternate mode 4 output 110 Alternate mode 5 output 111 Alternate mode 6 output
SW_MUX_CTL[27:24] SW_MUX_CTL[19:16] SW_MUX_CTL[11:8] SW_MUX_CTL[3:0]	mux2_in, mux1_in, func_in, gpio_psr/isr	**MUX Input Selection** 0000 No inputs selected 0001 GPIO PSR/ISR input 0010 Functional input 0100 Alternate Mode 1 input 1000 Alternate Mode 2 input 0011 Not recommended 0101 Not recommended 0110 Not recommended 0111 Not recommended 1001 Not recommended 1010 Not recommended 1011 Not recommended 1100 Not recommended 1101 Not recommended 1110 Not recommended 1111 Not recommended

4.3.4 Register Descriptions for SW Mux Control (SW_MUX_CTL)

Figure 4-6 through Figure 4-87 show the sw_mux_ctl registers. The functional multiplexing information shown in Table 4-8 enables the user to select the function of each I/O line by configuring the GPR or appropriate SW_MUX_CTL registers. The data in the table applies to any I/O that is multiplexed to provide different functions.

Additional information about EMI Multiplexing is shown in Table 4-13.

Absolute: 0x43FA_C00C Access: User Read/Write

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R		sw_mux_ctl_cspi3_miso								sw_mux_ctl_cspi3_sclk						
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R		sw_mux_ctl_cspi3_spi_rdy								sw_mux_ctl_ttm_pad						
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	1	0	0	1	0

Figure 4-6. Register Description sw_mux_ctl_cspi3_miso_cspi3_sclk_cspi3_spi_rdy_ttm_pad

Absolute: 0x43FA_C010 Access: User Read/Write

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R		sw_mux_ctl_ata_reset_b								sw_mux_ctl_ce_control						
W																
Reset	0	0	0	0	0	0	0	1	0	0	0	1	0	0	1	0

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R		sw_mux_ctl_clkss								sw_mux_ctl_cspi3_mosi						
W																
Reset	0	0	0	1	0	0	1	0	0	0	0	0	0	0	0	0

Figure 4-7. Register Description sw_mux_ctl_ata_reset_b_ce_control_clkss_cspi3_mosi

Absolute: 0x43FA_C014 Access: User Read/Write

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R		sw_mux_ctl_ata_cs1								sw_mux_ctl_ata_dior						
W																
Reset	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	1

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R		sw_mux_ctl_ata_diow								sw_mux_ctl_ata_dmack						
W																
Reset	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	1

Figure 4-8. Register Description sw_mux_ctl_ata_cs1_ata_dior_ata_diow_ata_dmack

Absolute: 0x43FA_C018 Access: User Read/Write

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R		sw_mux_ctl_sd1_data1								sw_mux_ctl_sd1_data2						
W																
Reset	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	1

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R		sw_mux_ctl_sd1_data3								sw_mux_ctl_ata_cs0						
W																
Reset	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	1

Figure 4-9. Register Description sw_mux_ctl_sd1_data1_sd1_data2_sd1_data3_ata_cs0

Absolute: 0x43FA_C01C Access: User Read/Write

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R		sw_mux_ctl_d3_spl								sw_mux_ctl_sd1_cmd						
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R		sw_mux_ctl_sd1_clk								sw_mux_ctl_sd1_data0						
W																
Reset	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	1

Figure 4-10. Register Description sw_mux_ctl_d3_spl_sd1_cmd_sd1_clk_sd1_data0

Absolute: 0x43FA_C020 Access: User Read/Write

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R		sw_mux_ctl_vsync3								sw_mux_ctl_contrast						
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R		sw_mux_ctl_d3_rev								sw_mux_ctl_d3_cls						
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Figure 4-11. Register Description sw_mux_ctl_vsync3_contrast_d3_rev_d3_cls

Absolute: 0x43FA_C024 Access: User Read/Write

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R		sw_mux_ctl_ser_rs								sw_mux_ctl_par_rs						
W																
Reset	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R		sw_mux_ctl_write								sw_mux_ctl_read						
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Figure 4-12. Register Description sw_mux_ctl_ser_rs_par_rs_write_read

Absolute: 0x43FA_C028 Access: User Read/Write

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R		sw_mux_ctl_sd_d_io								sw_mux_ctl_sd_d_clk						
W																
Reset	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	1

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R		sw_mux_ctl_lcs0								sw_mux_ctl_lcs1						
W																
Reset	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	1

Figure 4-13. Register Description sw_mux_ctl_sd_d_io_sd_d_clk_lcs0_lcs1

Absolute: 0x43FA_C02C Access: User Read/Write

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R		sw_mux_ctl_hsync								sw_mux_ctl_fpshift						
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R		sw_mux_ctl_drdy0								sw_mux_ctl_sd_d_i						
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Figure 4-14. Register Description sw_mux_ctl_hsync_fpshift_drdy0_sd_d_i

Absolute: 0x43FA_C030 Access: User Read/Write

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R		sw_mux_ctl_ld15								sw_mux_ctl_ld16						
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R		sw_mux_ctl_ld17								sw_mux_ctl_vsync0						
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Figure 4-15. Register Description sw_mux_ctl_ld15_ld16_ld17_vsync0

Absolute: 0x43FA_C034 Access: User Read/Write

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R		sw_mux_ctl_ld11								sw_mux_ctl_ld12						
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R		sw_mux_ctl_ld13								sw_mux_ctl_ld14						
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Figure 4-16. Register Description sw_mux_ctl_ld11_ld12_ld13_ld14

Absolute: 0x43FA_C038 Access: User Read/Write

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R		sw_mux_ctl_ld7								sw_mux_ctl_ld8						
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R		sw_mux_ctl_ld9								sw_mux_ctl_ld10						
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Figure 4-17. Register Description sw_mux_ctl_ld7_ld8_ld9_ld10

Absolute: 0x43FA_C03C Access: User Read/Write

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R		sw_mux_ctl_ld3								sw_mux_ctl_ld4						
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R		sw_mux_ctl_ld5								sw_mux_ctl_ld6						
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Figure 4-18. Register Description sw_mux_ctl_ld3_ld4_ld5_ld6

Absolute: 0x43FA_C040 Access: User Read/Write

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R		sw_mux_ctl_usbh2_data1								sw_mux_ctl_ld0						
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R		sw_mux_ctl_ld1								sw_mux_ctl_ld2						
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Figure 4-19. Register Description sw_mux_ctl_usbh2_data1_ld0_ld1_ld2

Absolute: 0x43FA_C044 Access: User Read/Write

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R		sw_mux_ctl_usbh2_dir								sw_mux_ctl_usbh2_stp						
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R		sw_mux_ctl_usbh2_nxt								sw_mux_ctl_usbh2_data0						
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Figure 4-20. Register Description sw_mux_ctl_usbh2_dir_usbh2_stp_usbh2_nxt_usbh2_data0

Absolute: 0x43FA_C048 Access: User Read/Write

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R		sw_mux_ctl_usbotg_data5								sw_mux_ctl_usbotg_data6						
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R		sw_mux_ctl_usbotg_data7								sw_mux_ctl_usbh2_clk						
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Figure 4-21. Register Description sw_mux_ctl_usbotg_data5_usbotg_data6_usbotg_data7_usbh2_clk

Absolute: 0x43FA_C04C Access: User Read/Write

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R		sw_mux_ctl_usbotg_data1								sw_mux_ctl_usbotg_data2						
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R		sw_mux_ctl_usbotg_data3								sw_mux_ctl_usbotg_data4						
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Figure 4-22. Register Description sw_mux_ctl_usbotg_data1_usbotg_data2_usbotg_data3_usbotg_data4

Absolute: 0x43FA_C050 Access: User Read/Write

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R		sw_mux_ctl_usbotg_dir								sw_mux_ctl_usbotg_stp						
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R		sw_mux_ctl_usbotg_nxt								sw_mux_ctl_usbotg_data0						
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Figure 4-23. Register Description sw_mux_ctl_usbotg_dir_usbotg_stp_usbotg_nxt_usbotg_data0

Absolute: 0x43FA_C054 Access: User Read/Write

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R		sw_mux_ctl_usb_pwr								sw_mux_ctl_usb_oc						
W																
Reset	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	1

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R		sw_mux_ctl_usb_byp								sw_mux_ctl_usbotg_clk						
W																
Reset	0	0	0	1	0	0	1	0	0	0	0	0	0	0	0	0

Figure 4-24. Register Description sw_mux_ctl_usb_pwr_usb_oc_usb_byp_usbotg_clk

Absolute: 0x43FA_C058 Access: User Read/Write

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R		sw_mux_ctl_tdo								sw_mux_ctl_trstb						
W																
Reset	0	0	0	1	0	0	1	0	0	0	0	1	0	0	1	0

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R				$\overline{\text{sw\_mux\_ctl\_de}}$						sw_mux_ctl_sjc_mod						
W																
Reset	0	0	0	1	0	0	1	0	0	0	0	1	0	0	1	0

Figure 4-25. Register Description sw_mux_ctl_tdo_trstb_de_b_sjc_mod

Absolute: 0x43FA_C05C Access: User Read/Write

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R		sw_mux_ctl_rtck								sw_mux_ctl_tck						
W																
Reset	0	0	0	1	0	0	1	0	0	0	0	1	0	0	1	0

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R		sw_mux_ctl_tms								sw_mux_ctl_tdi						
W																
Reset	0	0	0	1	0	0	1	0	0	0	0	1	0	0	1	0

Figure 4-26. Register Description sw_mux_ctl_rtck_tck_tms_tdi

Absolute: 0x43FA_C060 Access: User Read/Write

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R		sw_mux_ctl_key_col4								sw_mux_ctl_key_col5						
W																
Reset	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	1

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R		sw_mux_ctl_key_col6								sw_mux_ctl_key_col7						
W																
Reset	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	1

Figure 4-27. Register Description sw_mux_ctl_key_col4_key_col5_key_col6_key_col7

Absolute: 0x43FA_C064 Access: User Read/Write

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R		sw_mux_ctl_key_col0								sw_mux_ctl_key_col1						
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R		sw_mux_ctl_key_col2								sw_mux_ctl_key_col3						
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Figure 4-28. Register Description sw_mux_ctl_key_col0_key_col1_key_col2_key_col3

Absolute: 0x43FA_C068 Access: User Read/Write

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R		sw_mux_ctl_key_row4								sw_mux_ctl_key_row5						
W																
Reset	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	1

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R		sw_mux_ctl_key_row6								sw_mux_ctl_key_row7						
W																
Reset	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	1

Figure 4-29. Register Description sw_mux_ctl_key_row4_key_row5_key_row6_key_row7

Absolute: 0x43FA_C06C Access: User Read/Write

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R		sw_mux_ctl_key_row0								sw_mux_ctl_key_row1						
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R		sw_mux_ctl_key_row2								sw_mux_ctl_key_row3						
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Figure 4-30. Register Description sw_mux_ctl_key_row0_key_row1_key_row2_key_row3

Absolute: 0x43FA_C070 Access: User Read/Write

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R		sw_mux_ctl_txd2								sw_mux_ctl_rts2						
W																
Reset	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R		sw_mux_ctl_cts2								sw_mux_ctl_batt_line						
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Figure 4-31. Register Description sw_mux_ctl_txd2_rts2_cts2_batt_line

Absolute: 0x43FA_C074 Access: User Read/Write

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R		sw_mux_ctl_ri_dte1								sw_mux_ctl_dcd_dte1						
W																
Reset	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	1

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R		sw_mux_ctl_dtr_dce2								sw_mux_ctl_rxd2						
W																
Reset	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	1

Figure 4-32. Register Description sw_mux_ctl_ri_dte1_dcd_dte1_dtr_dce2_rxd2

Absolute: 0x43FA_C078 Access: User Read/Write

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R		sw_mux_ctl_ri_dce1								sw_mux_ctl_dcd_dce1						
W																
Reset	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	1

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R		sw_mux_ctl_dtr_dte1								sw_mux_ctl_dsr_dte1						
W																
Reset	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	1

Figure 4-33. Register Description sw_mux_ctl_ri_dce1_dcd_dce1_dtr_dte1_dsr_dte1

Absolute: 0x43FA_C07C Access: User Read/Write

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R		sw_mux_ctl_rts1								sw_mux_ctl_cts1						
W																
Reset	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	1

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R		sw_mux_ctl_dtr_dce1								sw_mux_ctl_dsr_dce1						
W																
Reset	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	1

Figure 4-34. Register Description sw_mux_ctl_rts1_cts1_dtr_dce1_dsr_dce1

Absolute: 0x43FA_C080 Access: User Read/Write

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R		sw_mux_ctl_cspi2_sclk								sw_mux_ctl_cspi2_spi_rdy						
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R		sw_mux_ctl_rxd1								sw_mux_ctl_txd1						
W																
Reset	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	1

Figure 4-35. Register Description sw_mux_ctl_cspi2_sclk_cspi2_spi_rdy_rxd1_txd1

Absolute: 0x43FA_C084 Access: User Read/Write

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R		sw_mux_ctl_cspi2_miso								sw_mux_ctl_cspi2_ss0						
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R		sw_mux_ctl_cspi2_ss1								sw_mux_ctl_cspi2_ss2						
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Figure 4-36. Register Description sw_mux_ctl_cspi2_miso_cspi2_ss0_cspi2_ss1_cspi2_ss2

Absolute: 0x43FA_C088 Access: User Read/Write

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R		sw_mux_ctl_cspi1_ss2								sw_mux_ctl_cspi1_sclk						
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R		sw_mux_ctl_cspi1_spi_rdy								sw_mux_ctl_cspi2_mosi						
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Figure 4-37. Register Description sw_mux_ctl_cspi1_ss2_cspi1_sclk_cspi1_spi_rdy_cspi2_mosi

Absolute: 0x43FA_C08C Access: User Read/Write

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R		sw_mux_ctl_cspi1_mosi								sw_mux_ctl_cspi1_miso						
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R		sw_mux_ctl_cspi1_ss0								sw_mux_ctl_cspi1_ss1						
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Figure 4-38. Register Description sw_mux_ctl_cspi1_mosi_cspi1_miso_cspi1_ss0_cspi1_ss1

Absolute: 0x43FA_C090 Access: User Read/Write

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R		sw_mux_ctl_stxd6								sw_mux_ctl_srxd6						
W																
Reset	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	1

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R		sw_mux_ctl_sck6								sw_mux_ctl_sfs6						
W																
Reset	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	1

Figure 4-39. Register Description sw_mux_ctl_stxd6_srxd6_sck6_sfs6

Absolute: 0x43FA_C094 Access: User Read/Write

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R		sw_mux_ctl_stxd5								sw_mux_ctl_srxd5						
W																
Reset	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	1

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R		sw_mux_ctl_sck5								sw_mux_ctl_sfs5						
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Figure 4-40. Register Description sw_mux_ctl_stxd5_srxd5_sck5_sfs5

Absolute: 0x43FA_C098 Access: User Read/Write

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R		sw_mux_ctl_stxd4								sw_mux_ctl_srxd4						
W																
Reset	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	1

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R		sw_mux_ctl_sck4								sw_mux_ctl_sfs4						
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Figure 4-41. Register Description sw_mux_ctl_stxd4_srxd4_sck4_sfs4

Absolute: 0x43FA_C09C Access: User Read/Write

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R		sw_mux_ctl_stxd3								sw_mux_ctl_srxd3						
W																
Reset	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	1

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R		sw_mux_ctl_sck3								sw_mux_ctl_sfs3						
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Figure 4-42. Register Description sw_mux_ctl_stxd3_srxd3_sck3_sfs3

Absolute: 0x43FA_C0A0 Access: User Read/Write

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R		sw_mux_ctl_csi_hsync								sw_mux_ctl_csi_pixclk						
W																
Reset	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	1

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R		sw_mux_ctl_i2c_clk								sw_mux_ctl_i2c_dat						
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Figure 4-43. Register Description sw_mux_ctl_csi_hsync_csi_pixclk_i2c_clk_i2c_dat

Absolute: 0x43FA_C0A4 Access: User Read/Write

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R		sw_mux_ctl_csi_d14								sw_mux_ctl_csi_d15						
W																
Reset	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	1

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R		sw_mux_ctl_csi_mclk								sw_mux_ctl_csi_vsync						
W																
Reset	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	1

Figure 4-44. Register Description sw_mux_ctl_csi_d14_csi_d15_csi_mclk_csi_vsync

Absolute: 0x43FA_C0A8 Access: User Read/Write

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R		sw_mux_ctl_csi_d10								sw_mux_ctl_csi_d11						
W																
Reset	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	1

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R		sw_mux_ctl_csi_d12								sw_mux_ctl_csi_d13						
W																
Reset	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	1

Figure 4-45. Register Description sw_mux_ctl_csi_d10_csi_d11_csi_d12_csi_d13

Absolute: 0x43FA_C0AC Access: User Read/Write

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R		sw_mux_ctl_csi_d6								sw_mux_ctl_csi_d7						
W																
Reset	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	1

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R		sw_mux_ctl_csi_d8								sw_mux_ctl_csi_d9						
W																
Reset	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	1

Figure 4-46. Register Description sw_mux_ctl_csi_d6_csi_d7_csi_d8_csi_d9

Absolute: 0x43FA_C0B0 Access: User Read/Write

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R		sw_mux_ctl_m_request								sw_mux_ctl_m_grant						
W																
Reset	0	0	0	1	0	0	1	0	0	0	0	1	0	0	1	0

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R		sw_mux_ctl_csi_d4								sw_mux_ctl_csi_d5						
W																
Reset	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	1

Figure 4-47. Register Description sw_mux_ctl_m_request_m_grant_csi_d4_csi_d5

Absolute: 0x43FA_C0B4 Access: User Read/Write

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R		sw_mux_ctl_pc_rst								sw_mux_ctl_iois16						
W																
Reset	0	0	0	1	0	0	1	0	0	0	0	0	0	0	0	0

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R		sw_mux_ctl_pc_rw_b								sw_mux_ctl_pc_poe						
W																
Reset	0	0	0	1	0	0	1	0	0	0	0	1	0	0	1	0

Figure 4-48. Register Description sw_mux_ctl_pc_rst_iois16_pc_rw_b_pc_poe

Absolute: 0x43FA_C0B8 Access: User Read/Write

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R		sw_mux_ctl_pc_vs1								sw_mux_ctl_pc_vs2						
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R		sw_mux_ctl_pc_bvd1								sw_mux_ctl_pc_bvd2						
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Figure 4-49. Register Description sw_mux_ctl_pc_vs1_pc_vs2_pc_bvd1_pc_bvd2

Absolute: 0x43FA_C0BC Access: User Read/Write

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R		sw_mux_ctl_pc_cd2_b								sw_mux_ctl_pc_wait_b						
W																
Reset	0	0	0	1	0	0	1	0	0	0	0	0	0	0	0	0

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R		sw_mux_ctl_pc_ready								sw_mux_ctl_pc_pwron						
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Figure 4-50. Register Description sw_mux_ctl_pc_cd2_b_pc_wait_b_pc_ready_pc_pwron

Absolute: 0x43FA_C0C0 Access: User Read/Write

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R		sw_mux_ctl_d2								sw_mux_ctl_d1						
W																
Reset	0	0	0	1	0	0	1	0	0	0	0	1	0	0	1	0

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R		sw_mux_ctl_d0								sw_mux_ctl_pc_cd1_b						
W																
Reset	0	0	0	1	0	0	1	0	0	0	0	1	0	0	1	0

Figure 4-51. Register Description sw_mux_ctl_d2_d1_d0_pc_cd1_b

Absolute: 0x43FA_C0C4 Access: User Read/Write

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R		sw_mux_ctl_d6								sw_mux_ctl_d5						
W																
Reset	0	0	0	1	0	0	1	0	0	0	0	1	0	0	1	0

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R		sw_mux_ctl_d4								sw_mux_ctl_d3						
W																
Reset	0	0	0	1	0	0	1	0	0	0	0	1	0	0	1	0

Figure 4-52. Register Description sw_mux_ctl_d6_d5_d4_d3

Absolute: 0x43FA_C0C8 Access: User Read/Write

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R		sw_mux_ctl_d10								sw_mux_ctl_d9						
W																
Reset	0	0	0	1	0	0	1	0	0	0	0	1	0	0	1	0

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R		sw_mux_ctl_d8								sw_mux_ctl_d7						
W																
Reset	0	0	0	1	0	0	1	0	0	0	0	1	0	0	1	0

Figure 4-53. Register Description sw_mux_ctl_d10_d9_d8_d7

Absolute: 0x43FA_C0CC Access: User Read/Write

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R		sw_mux_ctl_d14								sw_mux_ctl_d13						
W																
Reset	0	0	0	1	0	0	1	0	0	0	0	1	0	0	1	0

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R		sw_mux_ctl_d12								sw_mux_ctl_d11						
W																
Reset	0	0	0	1	0	0	1	0	0	0	0	1	0	0	1	0

Figure 4-54. Register Description sw_mux_ctl_d14_d13_d12_d11

Absolute: 0x43FA_C0D0 Access: User Read/Write

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R		sw_mux_ctl_nfwp_b								sw_mux_ctl_nfce_b						
W																
Reset	0	0	0	1	0	0	1	0	0	0	0	1	0	0	1	0

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R		sw_mux_ctl_nfrb								sw_mux_ctl_d15						
W																
Reset	0	0	0	1	0	0	1	0	0	0	0	1	0	0	1	0

Figure 4-55. Register Description sw_mux_ctl_nfwp_b_nfce_b_nfrb_d15

Absolute: 0x43FA_C0D4 Access: User Read/Write

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R		sw_mux_ctl_nfwe_b								sw_mux_ctl_nfre_b						
W																
Reset	0	0	0	1	0	0	1	0	0	0	0	1	0	0	1	0

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R		sw_mux_ctl_nfale								sw_mux_ctl_nfcle						
W																
Reset	0	0	0	1	0	0	1	0	0	0	0	1	0	0	1	0

Figure 4-56. Register Description sw_mux_ctl_nfwe_b_nfre_b_nfale_nfcle

Absolute: 0x43FA_C0D8 Access: User Read/Write

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R		sw_mux_ctl_sdqs0								sw_mux_ctl_sdqs1						
W																
Reset	0	0	0	1	0	0	1	0	0	0	0	1	0	0	1	0

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R		sw_mux_ctl_sdqs2								sw_mux_ctl_sdqs3						
W																
Reset	0	0	0	1	0	0	1	0	0	0	0	1	0	0	1	0

Figure 4-57. Register Description sw_mux_ctl_sdqs0_sdqs1_sdqs2_sdqs3

Absolute: 0x43FA_C0DC Access: User Read/Write

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R		sw_mux_ctl_sdcke0								sw_mux_ctl_sdcke1						
W																
Reset	0	0	0	1	0	0	1	0	0	0	0	1	0	0	1	0

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R		sw_mux_ctl_sdclk*								Reserved						
W																
Reset	0	0	0	1	0	0	1	0	0	0	0	1	0	0	1	0

*Bits 8–14 control the differential output pair SDCLK and $\overline{\text{SDCLK}}$.

Figure 4-58. Register Description sw_mux_ctl_sdcke0_sdcke1_sdclk_sdclk_b

Absolute: 0x43FA_C0E0 Access: User Read/Write

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R		sw_mux_ctl_rw								sw_mux_ctl_ras						
W																
Reset	0	0	0	1	0	0	1	0	0	0	0	1	0	0	1	0

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R		sw_mux_ctl_cas								sw_mux_ctl_sdwe						
W																
Reset	0	0	0	1	0	0	1	0	0	0	0	1	0	0	1	0

Figure 4-59. Register Description sw_mux_ctl_rw_ras_cas_sdwe

Absolute: 0x43FA_C0E4 Access: User Read/Write

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R		sw_mux_ctl_cs5								sw_mux_ctl_ecb						
W																
Reset	0	0	0	1	0	0	1	0	0	0	0	1	0	0	1	0

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R		sw_mux_ctl_lba								sw_mux_ctl_bclk						
W																
Reset	0	0	0	1	0	0	1	0	0	0	0	1	0	0	1	0

Figure 4-60. Register Description sw_mux_ctl_cs5_ecb_lba_bclk

Absolute: 0x43FA_C0E8 Access: User Read/Write

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R		sw_mux_ctl_cs1								sw_mux_ctl_cs2						
W																
Reset	0	0	0	1	0	0	1	0	0	0	0	1	0	0	1	0

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R		sw_mux_ctl_cs3								sw_mux_ctl_cs4						
W																
Reset	0	0	0	1	0	0	1	0	0	0	0	1	0	0	1	0

Figure 4-61. Register Description sw_mux_ctl_cs1_cs2_cs3_cs4

Absolute: 0x43FA_C0EC Access: User Read/Write

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R		sw_mux_ctl_eb0								sw_mux_ctl_eb1						
W																
Reset	0	0	0	1	0	0	1	0	0	0	0	1	0	0	1	0

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R		sw_mux_ctl_oe								sw_mux_ctl_cs0						
W																
Reset	0	0	0	1	0	0	1	0	0	0	0	1	0	0	1	0

Figure 4-62. Register Description sw_mux_ctl_eb0_eb1_oe_cs0

Absolute: 0x43FA_C0F0 Access: User Read/Write

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R		sw_mux_ctl_dqm0								sw_mux_ctl_dqm1						
W																
Reset	0	0	0	1	0	0	1	0	0	0	0	1	0	0	1	0

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R		sw_mux_ctl_dqm2								sw_mux_ctl_dqm3						
W																
Reset	0	0	0	1	0	0	1	0	0	0	0	1	0	0	1	0

Figure 4-63. Register Description sw_mux_ctl_dqm0_dqm1_dqm2_dqm3

Absolute: 0x43FA_C0F4 Access: User Read/Write

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R		sw_mux_ctl_sd28								sw_mux_ctl_sd29						
W																
Reset	0	0	0	1	0	0	1	0	0	0	0	1	0	0	1	0

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R		sw_mux_ctl_sd30								sw_mux_ctl_sd31						
W																
Reset	0	0	0	1	0	0	1	0	0	0	0	1	0	0	1	0

Figure 4-64. Register Description sw_mux_ctl_sd28_sd29_sd30_sd31

Absolute: 0x43FA_C0F8 Access: User Read/Write

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R		sw_mux_ctl_sd24								sw_mux_ctl_sd25						
W																
Reset	0	0	0	1	0	0	1	0	0	0	0	1	0	0	1	0

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R		sw_mux_ctl_sd26								sw_mux_ctl_sd27						
W																
Reset	0	0	0	1	0	0	1	0	0	0	0	1	0	0	1	0

Figure 4-65. Register Description sw_mux_ctl_sd24_sd25_sd26_sd27

Absolute: 0x43FA_C0FC Access: User Read/Write

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R		sw_mux_ctl_sd20								sw_mux_ctl_sd21						
W																
Reset	0	0	0	1	0	0	1	0	0	0	0	1	0	0	1	0

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R		sw_mux_ctl_sd22								sw_mux_ctl_sd23						
W																
Reset	0	0	0	1	0	0	1	0	0	0	0	1	0	0	1	0

Figure 4-66. Register Description sw_mux_ctl_sd20_sd21_sd22_sd23

Absolute: 0x43FA_C100 Access: User Read/Write

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R		sw_mux_ctl_sd16								sw_mux_ctl_sd17						
W																
Reset	0	0	0	1	0	0	1	0	0	0	0	1	0	0	1	0

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R		sw_mux_ctl_sd18								sw_mux_ctl_sd19						
W																
Reset	0	0	0	1	0	0	1	0	0	0	0	1	0	0	1	0

Figure 4-67. Register Description sw_mux_ctl_sd16_sd17_sd18_sd19

Absolute: 0x43FA_C104 Access: User Read/Write

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R		sw_mux_ctl_sd12								sw_mux_ctl_sd13						
W																
Reset	0	0	0	1	0	0	1	0	0	0	0	1	0	0	1	0

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R		sw_mux_ctl_sd14								sw_mux_ctl_sd15						
W																
Reset	0	0	0	1	0	0	1	0	0	0	0	1	0	0	1	0

Figure 4-68. Register Description sw_mux_ctl_sd12_sd13_sd14_sd15

Absolute: 0x43FA_C108 Access: User Read/Write

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R		sw_mux_ctl_sd8								sw_mux_ctl_sd9						
W																
Reset	0	0	0	1	0	0	1	0	0	0	0	1	0	0	1	0

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R		sw_mux_ctl_sd10								sw_mux_ctl_sd11						
W																
Reset	0	0	0	1	0	0	1	0	0	0	0	1	0	0	1	0

Figure 4-69. Register Description sw_mux_ctl_sd8_sd9_sd10_sd11

Absolute: 0x43FA_C10C Access: User Read/Write

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R		sw_mux_ctl_sd4								sw_mux_ctl_sd5						
W																
Reset	0	0	0	1	0	0	1	0	0	0	0	1	0	0	1	0

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R		sw_mux_ctl_sd6								sw_mux_ctl_sd7						
W																
Reset	0	0	0	1	0	0	1	0	0	0	0	1	0	0	1	0

Figure 4-70. Register Description sw_mux_ctl_sd4_sd5_sd6_sd7

Absolute: 0x43FA_C110 Access: User Read/Write

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R		sw_mux_ctl_sd0								sw_mux_ctl_sd1						
W																
Reset	0	0	0	1	0	0	1	0	0	0	0	1	0	0	1	0

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R		sw_mux_ctl_sd2								sw_mux_ctl_sd3						
W																
Reset	0	0	0	1	0	0	1	0	0	0	0	1	0	0	1	0

Figure 4-71. Register Description sw_mux_ctl_sd0_sd1_sd2_sd3

Absolute: 0x43FA_C114 Access: User Read/Write

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R		sw_mux_ctl_a24								sw_mux_ctl_a25						
W																
Reset	0	0	0	1	0	0	1	0	0	0	0	1	0	0	1	0

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R		sw_mux_ctl_sdba1								sw_mux_ctl_sdba0						
W																
Reset	0	0	0	1	0	0	1	0	0	0	0	1	0	0	1	0

Figure 4-72. Register Description sw_mux_ctl_a24_a25_sdba1_sdba0

Absolute: 0x43FA_C118 Access: User Read/Write

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R		sw_mux_ctl_a20								sw_mux_ctl_a21						
W																
Reset	0	0	0	1	0	0	1	0	0	0	0	1	0	0	1	0

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R		sw_mux_ctl_a22								sw_mux_ctl_a23						
W																
Reset	0	0	0	1	0	0	1	0	0	0	0	1	0	0	1	0

Figure 4-73. Register Description sw_mux_ctl_a20_a21_a22_a23

Absolute: 0x43FA_C11C Access: User Read/Write

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R		sw_mux_ctl_a16								sw_mux_ctl_a17						
W																
Reset	0	0	0	1	0	0	1	0	0	0	0	1	0	0	1	0

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R		sw_mux_ctl_a18								sw_mux_ctl_a19						
W																
Reset	0	0	0	1	0	0	1	0	0	0	0	1	0	0	1	0

Figure 4-74. Register Description sw_mux_ctl_a16_a17_a18_a19

Absolute: 0x43FA_C120 Access: User Read/Write

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R		sw_mux_ctl_a12								sw_mux_ctl_a13						
W																
Reset	0	0	0	1	0	0	1	0	0	0	0	1	0	0	1	0

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R		sw_mux_ctl_a14								sw_mux_ctl_a15						
W																
Reset	0	0	0	1	0	0	1	0	0	0	0	1	0	0	1	0

Figure 4-75. Register Description sw_mux_ctl_a12_a13_a14_a15

Absolute: 0x43FA_C124 Access: User Read/Write

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R		sw_mux_ctl_a9								sw_mux_ctl_a10						
W																
Reset	0	0	0	1	0	0	1	0	0	0	0	1	0	0	1	0

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R		sw_mux_ctl_ma10								sw_mux_ctl_a11						
W																
Reset	0	0	0	1	0	0	1	0	0	0	0	1	0	0	1	0

Figure 4-76. Register Description sw_mux_ctl_a9_a10_ma10_a11

Absolute: 0x43FA_C128 Access: User Read/Write

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R		sw_mux_ctl_a5								sw_mux_ctl_a6						
W																
Reset	0	0	0	1	0	0	1	0	0	0	0	1	0	0	1	0

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R		sw_mux_ctl_a7								sw_mux_ctl_a8						
W																
Reset	0	0	0	1	0	0	1	0	0	0	0	1	0	0	1	0

Figure 4-77. Register Description sw_mux_ctl_a5_a6_a7_a8

Absolute: 0x43FA_C12C Access: User Read/Write

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R		sw_mux_ctl_a1								sw_mux_ctl_a2						
W																
Reset	0	0	0	1	0	0	1	0	0	0	0	1	0	0	1	0

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R		sw_mux_ctl_a3								sw_mux_ctl_a4						
W																
Reset	0	0	0	1	0	0	1	0	0	0	0	1	0	0	1	0

Figure 4-78. Register Description sw_mux_ctl_a1_a2_a3_a4

Absolute: 0x43FA_C130 Access: User Read/Write

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R		sw_mux_ctl_dvfs1								sw_mux_ctl_vpg0						
W																
Reset	0	0	0	1	0	0	1	0	0	0	0	1	0	0	1	0

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R		sw_mux_ctl_vpg1								sw_mux_ctl_a0						
W																
Reset	0	0	0	1	0	0	1	0	0	0	0	1	0	0	1	0

Figure 4-79. Register Description sw_mux_ctl_dvfs1_vpg0_vpg1_a0

Absolute: 0x43FA_C134 Access: User Read/Write

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R		sw_mux_ctl_ckil								sw_mux_ctl_power_fail						
W																
Reset	0	0	0	1	0	0	1	0	0	0	0	1	0	0	1	0

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R		sw_mux_ctl_vstby								sw_mux_ctl_dvfs0						
W																
Reset	0	0	0	1	0	0	1	0	0	0	0	1	0	0	1	0

Figure 4-80. Register Description sw_mux_ctl_ckil_power_fail_vstby_dvfs0

Absolute: 0x43FA_C138 Access: User Read/Write

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R		sw_mux_ctl_boot_mode1								sw_mux_ctl_boot_mode2						
W																
Reset	0	0	0	1	0	0	1	0	0	0	0	1	0	0	1	0

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R		sw_mux_ctl_boot_mode3								sw_mux_ctl_boot_mode4						
W																
Reset	0	0	0	1	0	0	1	0	0	0	0	1	0	0	1	0

Figure 4-81. Register Description sw_mux_ctl_boot_mode1_boot_mode2_boot_mode3_boot_mode4

Absolute: 0x43FA_C13C Access: User Read/Write

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R		sw_mux_ctl_reset_in_b								sw_mux_ctl_por_b						
W																
Reset	0	0	0	1	0	0	1	0	0	0	0	1	0	0	1	0

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R		sw_mux_ctl_clko								sw_mux_ctl_boot_mode0						
W																
Reset	0	0	0	1	0	0	1	0	0	0	0	1	0	0	1	0

Figure 4-82. Register Description sw_mux_ctl_reset_in_b_por_b_clko_boot_mode0

Absolute: 0x43FA_C140 Access: User Read/Write

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R		sw_mux_ctl_stx0								sw_mux_ctl_srx0						
W																
Reset	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	1

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R		sw_mux_ctl_simpd0								sw_mux_ctl_ckih						
W																
Reset	0	0	0	0	0	0	0	1	0	0	0	1	0	0	1	0

Figure 4-83. Register Description sw_mux_ctl_stx0_srx0_simpd0_ckih

Absolute: 0x43FA_C144 Access: User Read/Write

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R		sw_mux_ctl_gpio3_1								sw_mux_ctl_sclk0						
W																
Reset	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	1

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R		sw_mux_ctl_srst0								sw_mux_ctl_sven0						
W																
Reset	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	1

Figure 4-84. Register Description sw_mux_ctl_gpio3_1_sclk0_srst0_sven0

Absolute: 0x43FA_C148 Access: User Read/Write

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R		sw_mux_ctl_gpio1_4								sw_mux_ctl_gpio1_5						
W																
Reset	0	0	0	0	0	0	0	1	0	0	0	1	0	0	1	0

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R		sw_mux_ctl_gpio1_6								sw_mux_ctl_gpio3_0						
W																
Reset	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	1

Figure 4-85. Register Description sw_mux_ctl_gpio1_4_gpio1_5_gpio1_6_gpio3_0

Absolute: 0x43FA_C14C Access: User Read/Write

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R		sw_mux_ctl_gpio1_0								sw_mux_ctl_gpio1_1						
W																
Reset	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	1

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R		sw_mux_ctl_gpio1_2								sw_mux_ctl_gpio1_3						
W																
Reset	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	1

Figure 4-86. Register Description sw_mux_ctl_gpio1_0_gpio1_1_gpio1_2_gpio1_3

Absolute: 0x43FA_C150 Access: User Read/Write

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R		sw_mux_ctl_capture								sw_mux_ctl_compare						
W																
Reset	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	1

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R		sw_mux_ctl_watchdog_rst								sw_mux_ctl_pwmo						
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Figure 4-87. Register Description sw_mux_ctl_capture_compare_watchdog_rst_pwmo

4.3.5 Functional Multiplexing Modes

The IOMUX has four configurable modes: Hardware, Functional, Alternate, and GPIO. Each mode has a priority. Setting an I/O with a higher priority overrides the previous mode setting. Likewise, if a priority setting being applied is a lower priority than the priority of the current mode, the new mode setting is ignored. Table 4-7 shows the priority for each of the modes.

Table 4-7. Multiplexing Priorities

Priority	Mode
1	Hardware mode 2
2	Hardware mode 1
3	Alternate mode 2
4	Alternate mode 1
5	Functional mode

The four multiplexing modes are defined in the following sections.

4.3.5.1 Hardware Mode

This mode is used to set multiple sets of I/O signals by setting or clearing a single bit in the General Purpose Register (GPR).

4.3.5.2 Functional Mode

This is the primary mode of the I/O line. Like a default setting, the primary mode routes the signals for which it is named. For example, the functional mode of the RXD1 I/O line routes the RXD signal of UART1 to the external contact of the IC.

4.3.5.3 Alternate Modes

Each I/O has software-programmable bits that can select between the functional mode and other I/O muxing options. Each I/O signal has the potential of six alternate modes which are individually defined by software. For example, using an alternate mode allows the RXD signal to be routed to RI_DCE1 I/O. The six alternate mode options are as follows:

- Alternate Mode 1–2 (I/O)
- Alternate Modes 3–6 (output only)

4.3.5.4 GPIO Mode

In GPIO mode, configuration of the I/O is controlled by the GPIO module. For example, in the GPIO column of Table 4-8, MCU indicates MCU1_7, which is associated with GPIO1 bit 7.

Table 4-8. Functional Multiplexing Configuration

Contact Name	Group	Description	Configured by GPR		SW_MUX_CTL Bits	Configured by SW_MUX_CTL							
			Hardware Mode 1	Hardware Mode 2		Functional Mode	Alternate Mode 1	Alternate Mode 2	Alternate Mode 3	Alternate Mode 4	Alternate Mode 5	Alternate Mode 6	GPIO Mode
CAPTURE	Timer	Timer1 input capture, GPIO suggested for memstick1 card detect	ATA_DATA 14	—	sw_mux_ctl _capture [6:0]	Capture1	—	Compar e2	—	—	—	—	MCU1_7
COMPARE	Timer	Timer1 output compare, GPIO suggested for memstick2 card detect	ATA_DATA 15	—	sw_mux_ctl _compare [6:0]	Compare1	Captu re2	Compar e3	—	EPIT1	EPIT2	—	MCU1_8
WATCHDOG_ RST	WTDG	Watchdog reset output	—	—	sw_mux_ctl _watchdog _rst[6:0]	WDOG Reset	—	CSI Flash strobe	—	—	—	—	—
PWMO	PWM	PWM output	ATA_ IORDY	—	sw_mux_ctl _pwmo[6:0]	PWM Out	PC spkr out	—	—	—	—	—	MCU1_9
GPIO1_0	GPIO	GPIO1, bit 0	—	—	sw_mux_ctl _gpio1_0 [6:0]	—	ext DMA 0	—	—	—	—	—	MCU1_0
GPIO1_1	GPIO	GPIO1, bit 1	—	—	sw_mux_ctl _gpio1_1 [6:0]	—	ext DMA 1	—	—	—	—	—	MCU1_1
GPIO1_2	GPIO	GPIO1, bit 2	—	—	sw_mux_ctl _gpio1_2 [6:0]	—	ext DMA 2	—	—	—	—	—	MCU1_2
GPIO1_3	GPIO	GPIO1, bit 3	—	—	sw_mux_ctl _gpio1_3 [6:0]	—	—	—	—	—	—	—	MCU1_3

Table 4-8. Functional Multiplexing Configuration (continued)

Contact Name	Group	Description	Configured by GPR		SW_MUX_CTL Bits	Configured by SW_MUX_CTL							
			Hardware Mode 1	Hardware Mode 2		Functional Mode	Alternate Mode 1	Alternate Mode 2	Alternate Mode 3	Alternate Mode 4	Alternate Mode 5	Alternate Mode 6	GPIO Mode
GPIO1_4	GPIO	GPIO1, bit 4	—	—	sw_mux_ctl_gpio1_4 [6:0]	—	USB Host1 SUSPEND	—	—	—	—	—	MCU1_4
GPIO1_5	GPIO	Reserved input for connect to power ready output of a power management IC	—	—	sw_mux_ctl_gpio1_5 [6:0]	Power Ready Input	—	—	—	—	—	—	MCU1_5
GPIO1_6	GPIO	GPIO suggested for Tamper detect input	TAMPER_DETECT	—	sw_mux_ctl_gpio1_6 [6:0]	—	—	—	—	—	—	—	MCU1_6
GPIO3_0	GPIO	GPIO suggested as IPU CSI chip select3	SPLL_BYPASS_CLK	—	sw_mux_ctl_gpio3_0 [6:0]	—	—	—	—	—	—	—	MCU3_0
GPIO3_1	GPIO	GPIO suggested as IPU CSI chip select4	UPLL_BYPASS_CLK	—	sw_mux_ctl_gpio3_1 [6:0]	—	—	—	—	—	—	—	MCU3_1
SCLK0	SIM	SIM Port 0	—	—	sw_mux_ctl_sclk0[6:0]	SCLK0	CTI_TRIG_IN_1_4	DISPB_D2_CS	—	—	—	—	MCU3_2
SRST0	SIM	SIM Port 0	—	—	sw_mux_ctl_srst0[6:0]	RST0	—	DISPB_D12_VSYNC	—	—	—	—	MCU3_3
SVEN0	SIM	SIM Port 0	—	—	sw_mux_ctl_sven0[6:0]	SVEN0	CTI_TRIG_IN_1_6	—	—	—	—	—	MCU2_0

Table 4-8. Functional Multiplexing Configuration (continued)

Contact Name	Group	Description	Configured by GPR		SW_MUX_CTL Bits	Configured by SW_MUX_CTL							
			Hardware Mode 1	Hardware Mode 2		Functional Mode	Alternate Mode 1	Alternate Mode 2	Alternate Mode 3	Alternate Mode 4	Alternate Mode 5	Alternate Mode 6	GPIO Mode
STX0	SIM	SIM Port 0	—	—	sw_mux_ctl_stx0[6:0]	DATA0_TX_OUT	CTI_TRIG_IN_1_5	—	—	—	—	—	MCU2_1
SRX0	SIM	SIM Port 0	—	—	sw_mux_ctl_srx0[6:0]	RCVD0_IN	—	—	—	—	—	—	MCU2_2
SIMPD0	SIM	SIM Port 0	—	—	sw_mux_ctl_simpd0[6:0]	SIMPD0	—	—	—	—	—	—	MCU2_3
CKIH	Clock and Reset and PM	High frequency clock input	—	—	—	CKIH	—	—	—	—	—	—	—
$\overline{\text{RESET\_IN}}$	Clock and Reset and PM	Master Reset Input	$\overline{\text{RESET\_IN}}$	—	sw_mux_ctl_reset_in_b[6:0]	—	—	—	—	—	—	—	—
$\overline{\text{POR}}$	Clock and Reset and PM	Power On Reset input	—	—	—	POR_B	—	—	—	—	—	—	—
CLKO	Clock and Reset and PM	Clock out signal	—	—	—	CCM_CLKO	—	—	—	—	—	—	—

Table 4-8. Functional Multiplexing Configuration (continued)

Contact Name	Group	Description	Configured by GPR		SW_MUX_CTL Bits	Configured by SW_MUX_CTL							
			Hardware Mode 1	Hardware Mode 2		Functional Mode	Alternate Mode 1	Alternate Mode 2	Alternate Mode 3	Alternate Mode 4	Alternate Mode 5	Alternate Mode 6	GPIO Mode
BOOT_MODE 0	Clock and Reset and PM	Boot Mode 0	—	—	—	BOOT0	—	—	—	—	—	—	—
BOOT_MODE 1	Clock and Reset and PM	Boot Mode 1	—	—	—	BOOT1	—	—	—	—	—	—	—
BOOT_MODE 2	Clock and Reset and PM	Boot Mode 2	—	—	—	BOOT2	—	—	—	—	—	—	—
BOOT_MODE 3	Clock and Reset and PM	Boot Mode 3	—	—	—	BOOT3	—	—	—	—	—	—	—
BOOT_MODE 4	Clock and Reset and PM	Boot Mode 4	—	—	—	BOOT4	—	—	—	—	—	—	—
CKIL	Clock and Reset and PM	Low frequency clock input	—	—	—	CKIL	—	—	—	—	—	—	—

Table 4-8. Functional Multiplexing Configuration (continued)

Contact Name	Group	Description	Configured by GPR		SW_MUX_CTL Bits	Configured by SW_MUX_CTL							
			Hardware Mode 1	Hardware Mode 2		Functional Mode	Alternate Mode 1	Alternate Mode 2	Alternate Mode 3	Alternate Mode 4	Alternate Mode 5	Alternate Mode 6	GPIO Mode
POWER_FAIL	Clock and Reset and PM	power shut-off input	—	—	—	POWER_FAIL	—	—	—	—	—	—	—
VSTBY	Clock and Reset and PM	Power management State retention output	—	—	sw_mux_ctl_vstby[6:0]	VSTBY	—	—	—	—	—	—	—
DVFS0	Clock and Reset and PM	Power management voltage change output	—	—	sw_mux_ctl_dvfs0[6:0]	DVFS0	—	—	—	—	—	—	—
DVFS1	Clock and Reset and PM	Power management voltage change output	—	—	sw_mux_ctl_dvfs1[6:0]	DVFS1	—	—	—	—	—	—	—
VPG0	Clock and Reset and PM	Power management power gating output for ARM	—	—	sw_mux_ctl_vpg0[6:0]	VPG0	—	—	—	—	—	—	—
VPG1	Clock and Reset and PM	Power management power gating output for the L2 Cache	—	—	sw_mux_ctl_vpg1[6:0]	VPG1	—	—	—	—	—	—	—
A0	EMI	EIM address 0	—	—	sw_mux_ctl_a0[6:0]	EMI_ADDR[0]	—	—	—	—	—	—	—

Table 4-8. Functional Multiplexing Configuration (continued)

Contact Name	Group	Description	Configured by GPR		SW_MUX_CTL Bits	Configured by SW_MUX_CTL							
			Hardware Mode 1	Hardware Mode 2		Functional Mode	Alternate Mode 1	Alternate Mode 2	Alternate Mode 3	Alternate Mode 4	Alternate Mode 5	Alternate Mode 6	GPIO Mode
A1	EMI	EIM address 1	—	—	sw_mux_ctl_a1[6:0]	EMI_ADDR[1]	—	—	—	—	—	—	—
A2	EMI	EIM address 2	—	—	sw_mux_ctl_a2[6:0]	EMI_ADDR[2]	—	—	—	—	—	—	—
A3	EMI	EIM address 3	—	—	sw_mux_ctl_a3[6:0]	EMI_ADDR[3]	—	—	—	—	—	—	—
A4	EMI	EIM address 4	—	—	sw_mux_ctl_a4[6:0]	EMI_ADDR[4]	—	—	—	—	—	—	—
A5	EMI	EIM address 5	—	—	sw_mux_ctl_a5[6:0]	EMI_ADDR[5]	—	—	—	—	—	—	—
A6	EMI	EIM address 6	—	—	sw_mux_ctl_a6[6:0]	EMI_ADDR[6]	—	—	—	—	—	—	—
A7	EMI	EIM address 7	—	—	sw_mux_ctl_a7[6:0]	EMI_ADDR[7]	—	—	—	—	—	—	—
A8	EMI	EIM address 8	—	—	sw_mux_ctl_a8[6:0]	EMI_ADDR[8]	—	—	—	—	—	—	—
A9	EMI	EIM address 9	—	—	sw_mux_ctl_a9[6:0]	EMI_ADDR[9]	—	—	—	—	—	—	—
A10	EMI	EIM address 10	—	—	sw_mux_ctl_a10[6:0]	EMI_ADDR[10]	—	—	—	—	—	—	—
MA10	EMI	SDRAM controller address 10	—	—	sw_mux_ctl_ma10[6:0]	M3IF_MA10	—	—	—	—	—	—	—
A11	EMI	EIM address 11	—	—	sw_mux_ctl_a11[6:0]	EMI_ADDR[11]	—	—	—	—	—	—	—
A12	EMI	EIM address 12	—	—	sw_mux_ctl_a12[6:0]	EMI_ADDR[12]	—	—	—	—	—	—	—

Table 4-8. Functional Multiplexing Configuration (continued)

Contact Name	Group	Description	Configured by GPR		SW_MUX_CTL Bits	Configured by SW_MUX_CTL							
			Hardware Mode 1	Hardware Mode 2		Functional Mode	Alternate Mode 1	Alternate Mode 2	Alternate Mode 3	Alternate Mode 4	Alternate Mode 5	Alternate Mode 6	GPIO Mode
A13	EMI	EIM address 13	—	—	sw_mux_ctl_a13[6:0]	EMI_ADDR[13]	—	—	—	—	—	—	—
A14	EMI	EIM address 14	—	—	sw_mux_ctl_a14[6:0]	EMI_ADDR[14]	—	—	—	—	—	—	—
A15	EMI	EIM address 15	—	—	sw_mux_ctl_a15[6:0]	EMI_ADDR[15]	—	—	—	—	—	—	—
A16	EMI	EIM address 16	—	—	sw_mux_ctl_a16[6:0]	EMI_ADDR[16]	—	—	—	—	—	—	—
A17	EMI	EIM address 17	—	—	sw_mux_ctl_a17[6:0]	EMI_ADDR[17]	—	—	—	—	—	—	—
A18	EMI	EIM address 18	—	—	sw_mux_ctl_a18[6:0]	EMI_ADDR[18]	—	—	—	—	—	—	—
A19	EMI	EIM address 19	—	—	sw_mux_ctl_a19[6:0]	EMI_ADDR[19]	—	—	—	—	—	—	—
A20	EMI	EIM address 20	—	—	sw_mux_ctl_a20[6:0]	EMI_ADDR[20]	—	—	—	—	—	—	—
A21	EMI	EIM address 21	—	—	sw_mux_ctl_a21[6:0]	EMI_ADDR[21]	—	—	—	—	—	—	—
A22	EMI	EIM address 22	—	—	sw_mux_ctl_a22[6:0]	EMI_ADDR[22]	—	—	—	—	—	—	—
A23	EMI	EIM address 23	—	—	sw_mux_ctl_a23[6:0]	EMI_ADDR[23]	—	—	—	—	—	—	—
A24	EMI	EIM address 24	—	—	sw_mux_ctl_a24[6:0]	EMI_ADDR[24]	—	—	—	—	—	—	—
A25	EMI	EIM address 25	—	—	sw_mux_ctl_a25[6:0]	EMI_ADDR[25]	—	—	—	—	—	—	—

Table 4-8. Functional Multiplexing Configuration (continued)

Contact Name	Group	Description	Configured by GPR		SW_MUX_CTL Bits	Configured by SW_MUX_CTL							
			Hardware Mode 1	Hardware Mode 2		Functional Mode	Alternate Mode 1	Alternate Mode 2	Alternate Mode 3	Alternate Mode 4	Alternate Mode 5	Alternate Mode 6	GPIO Mode
SDBA1	EMI	EIM Bank Address	—	—	sw_mux_ctl_sdba1 [6:0]	SDBA1	—	—	—	—	—	—	—
SDBA0	EMI	EIM Bank Address	—	—	sw_mux_ctl_sdba0 [6:0]	SDBA0	—	—	—	—	—	—	—
SD0	EMI	DDR/SDRAM Data 0	—	—	—	EMI_DATA[0]	—	—	—	—	—	—	—
SD1	EMI	DDR/SDRAM Data 1	—	—	—	EMI_DATA[1]	—	—	—	—	—	—	—
SD2	EMI	DDR/SDRAM Data 2	—	—	—	EMI_DATA[2]	—	—	—	—	—	—	—
SD3	EMI	DDR/SDRAM Data 3	—	—	—	EMI_DATA[3]	—	—	—	—	—	—	—
SD4	EMI	DDR/SDRAM Data 4	—	—	—	EMI_DATA[4]	—	—	—	—	—	—	—
SD5	EMI	DDR/SDRAM Data 5	—	—	—	EMI_DATA[5]	—	—	—	—	—	—	—
SD6	EMI	DDR/SDRAM Data 6	—	—	—	EMI_DATA[6]	—	—	—	—	—	—	—
SD7	EMI	DDR/SDRAM Data 7	—	—	—	EMI_DATA[7]	—	—	—	—	—	—	—
SD8	EMI	DDR/SDRAM Data 8	—	—	—	EMI_DATA[8]	—	—	—	—	—	—	—
SD9	EMI	DDR/SDRAM Data 9	—	—	—	EMI_DATA[9]	—	—	—	—	—	—	—
SD10	EMI	DDR/SDRAM Data 10	—	—	—	EMI_DATA[10]	—	—	—	—	—	—	—

Table 4-8. Functional Multiplexing Configuration (continued)

Contact Name	Group	Description	Configured by GPR		SW_MUX_ CTL Bits	Configured by SW_MUX_CTL							
			Hardware Mode 1	Hardware Mode 2		Functional Mode	Alternate Mode 1	Alternate Mode 2	Alternate Mode 3	Alternate Mode 4	Alternate Mode 5	Alternate Mode 6	GPIO Mode
SD11	EMI	DDR/SDRAM Data 11	—	—	—	EMI_DATA[11]	—	—	—	—	—	—	—
SD12	EMI	DDR/SDRAM Data 12	—	—	—	EMI_DATA[12]	—	—	—	—	—	—	—
SD13	EMI	DDR/SDRAM Data 13	—	—	—	EMI_DATA[13]	—	—	—	—	—	—	—
SD14	EMI	DDR/SDRAM Data 14	—	—	—	EMI_DATA[14]	—	—	—	—	—	—	—
SD15	EMI	DDR/SDRAM Data 15	—	—	—	EMI_DATA[15]	—	—	—	—	—	—	—
SD16	EMI	DDR/SDRAM Data 16	—	—	—	EMI_DATA[16]	—	—	—	—	—	—	—
SD17	EMI	DDR/SDRAM Data 17	—	—	—	EMI_DATA[17]	—	—	—	—	—	—	—
SD18	EMI	DDR/SDRAM Data 18	—	—	—	EMI_DATA[18]	—	—	—	—	—	—	—
SD19	EMI	DDR/SDRAM Data 19	—	—	—	EMI_DATA[19]	—	—	—	—	—	—	—
SD20	EMI	DDR/SDRAM Data 20	—	—	—	EMI_DATA[20]	—	—	—	—	—	—	—
SD21	EMI	DDR/SDRAM Data 21	—	—	—	EMI_DATA[21]	—	—	—	—	—	—	—
SD22	EMI	DDR/SDRAM Data 22	—	—	—	EMI_DATA[22]	—	—	—	—	—	—	—
SD23	EMI	DDR/SDRAM Data 23	—	—	—	EMI_DATA[23]	—	—	—	—	—	—	—

Table 4-8. Functional Multiplexing Configuration (continued)

Contact Name	Group	Description	Configured by GPR		SW_MUX_CTL Bits	Configured by SW_MUX_CTL							
			Hardware Mode 1	Hardware Mode 2		Functional Mode	Alternate Mode 1	Alternate Mode 2	Alternate Mode 3	Alternate Mode 4	Alternate Mode 5	Alternate Mode 6	GPIO Mode
SD24	EMI	DDR/SDRAM Data 24	—	—	—	EMI_DATA[24]	—	—	—	—	—	—	—
SD25	EMI	DDR/SDRAM Data 25	—	—	—	EMI_DATA[25]	—	—	—	—	—	—	—
SD26	EMI	DDR/SDRAM Data 26	—	—	—	EMI_DATA[26]	—	—	—	—	—	—	—
SD27	EMI	DDR/SDRAM Data 27	—	—	—	EMI_DATA[27]	—	—	—	—	—	—	—
SD28	EMI	DDR/SDRAM Data 28	—	—	—	EMI_DATA[28]	—	—	—	—	—	—	—
SD29	EMI	DDR/SDRAM Data 29	—	—	—	EMI_DATA[29]	—	—	—	—	—	—	—
SD30	EMI	DDR/SDRAM Data 30	—	—	—	EMI_DATA[30]	—	—	—	—	—	—	—
SD31	EMI	DDR/SDRAM Data 31	—	—	—	EMI_DATA[31]	—	—	—	—	—	—	—
DQM0	EMI	Byte strobe DDR data enable	—	—	sw_mux_ctl_dqm0[6:0]	DQM[0]	—	—	—	—	—	—	—
DQM1	EMI	Byte strobe DDR data enable	—	—	sw_mux_ctl_dqm1[6:0]	DQM[1]	—	—	—	—	—	—	—
DQM2	EMI	Byte strobe DDR data enable	—	—	sw_mux_ctl_dqm2[6:0]	DQM[2]	—	—	—	—	—	—	—
DQM3	EMI	Byte strobe DDR data enable	—	—	sw_mux_ctl_dqm3[6:0]	DQM[3]	—	—	—	—	—	—	—
EB0	EMI	LSB Byte strobe WEIM data enable; Controls D[7:0]	—	—	sw_mux_ctl_eb0[6:0]	EB_B[0]	—	—	—	—	—	—	—

Table 4-8. Functional Multiplexing Configuration (continued)

Contact Name	Group	Description	Configured by GPR		SW_MUX_CTL Bits	Configured by SW_MUX_CTL							
			Hardware Mode 1	Hardware Mode 2		Functional Mode	Alternate Mode 1	Alternate Mode 2	Alternate Mode 3	Alternate Mode 4	Alternate Mode 5	Alternate Mode 6	GPIO Mode
EB1	EMI	LSB Byte strobe WEIM data enable Controls D[15:8]	—	—	sw_mux_ctl_eb1[6:0]	EB_B[1]	—	—	—	—	—	—	—
OE	EMI	Memory Output enable	—	—	sw_mux_ctl_oe[6:0]	EMI_OE_B	—	—	—	—	—	—	—
CS0	EMI	Chip select 0	—	—	sw_mux_ctl_cs0[6:0]	WEIM_CS_B0	—	—	—	—	—	—	—
CS1	EMI	Chip select 1	—	—	sw_mux_ctl_cs1[6:0]	WEIM_CS_B1	—	—	—	—	—	—	—
CS2	EMI	Chip select 2/SDRAM Sync Flash chip select	—	—	sw_mux_ctl_cs2[6:0]	WEIM_CS_B2	—	—	—	—	—	—	—
CS3	EMI	Chip select 3/SDRAM Sync Flash chip select	—	—	sw_mux_ctl_cs3[6:0]	WEIM_CS_B3	—	—	—	—	—	—	—
CS4	EMI	Chip select 4	—	—	sw_mux_ctl_cs4[6:0]	WEIM_CS_B4	$\overline{\text{DTACK}}$	—	—	—	—	—	—
CS5	EMI	Chip select 5	—	—	sw_mux_ctl_cs5[6:0]	WEIM_CS_B5	—	—	—	—	—	—	—
ECB	EMI	End Current Burst	—	—	—	WEIM_ECB_B	—	—	—	—	—	—	—
LBA	EMI	Load Base Address	—	—	sw_mux_ctl_lba[6:0]	WEIM_LBA_B	—	—	—	—	—	—	—
BCLK	EMI	used by Flash for burst mode	—	—	sw_mux_ctl_bclk[6:0]	WEIM_BCLK	—	—	—	—	—	—	—
RW	EMI	read/write signal or WE for external dram	—	—	sw_mux_ctl_rw[6:0]	WEIM_RW_B	—	—	—	—	—	—	—
RAS	EMI	SDRAM row address select	—	—	sw_mux_ctl_ras[6:0]	M3IF_RAS_B	—	—	—	—	—	—	—

Table 4-8. Functional Multiplexing Configuration (continued)

Contact Name	Group	Description	Configured by GPR		SW_MUX_CTL Bits	Configured by SW_MUX_CTL							
			Hardware Mode 1	Hardware Mode 2		Functional Mode	Alternate Mode 1	Alternate Mode 2	Alternate Mode 3	Alternate Mode 4	Alternate Mode 5	Alternate Mode 6	GPIO Mode
CAS	EMI	SDRAM column address select	—	—	sw_mux_ctl_cas[6:0]	M3IF_CAS_B	—	—	—	—	—	—	—
SDWE	EMI	SDRAM write enable	—	—	sw_mux_ctl_sdwe[6:0]	SDRC_SDWE	—	—	—	—	—	—	—
SDCKE0	EMI	SDRAM clock enable0	—	—	sw_mux_ctl_sdcke0[6:0]	SDRC_SDCKE[0]	—	—	—	—	—	—	—
SDCKE1	EMI	SDRAM clock enable1	—	—	sw_mux_ctl_sdcke1[6:0]	SDRC_SDCKE[1]	—	—	—	—	—	—	—
SDCLK	EMI	SDRAM clock DDR clock pad	—	—	sw_mux_ctl_sdclk[6:0]	SDRC_SDCLK	—	—	—	—	—	—	—
SDCLK_B	DDR	False pad DDR_CLK	—	—	—	SDRC_SDCLK_B	—	—	—	—	—	—	—
SDQS0	EMI	DDR sample strobe	—	—	—	DQS[0]	—	—	—	—	—	—	—
SDQS1	EMI	DDR sample strobe	—	—	—	DQS[1]	—	—	—	—	—	—	—
SDQS2	EMI	DDR sample strobe	—	—	—	DQS[2]	—	—	—	—	—	—	—
SDQS3	EMI	DDR sample strobe	—	—	—	DQS[3]	—	—	—	—	—	—	—
$\overline{\text{NFWE}}$	EMI	NANDF write enable	ATA_DATA7	ATA_INTRQ	sw_mux_ctl_nfwe_b[6:0]	NFC_WE	—	USBH2 DATA2	—	TRACEDATA_0	—	—	MCU1_10
$\overline{\text{NFRE}}$	EMI	NANDF read enable	ATA_DATA8	ATA_BUFFER_EN	sw_mux_ctl_nfre_b[6:0]	NFC_RE	—	USBH2 DATA3	—	TRACEDATA_1	—	—	MCU1_11
NFALE	EMI	NANDF address latch enable	ATA_DATA9	ATA_DMARQ	sw_mux_ctl_nfale[6:0]	NFC_ALE	—	USBH2_DATA4	—	TRACEDATA_2	—	—	MCU1_12

Table 4-8. Functional Multiplexing Configuration (continued)

Contact Name	Group	Description	Configured by GPR		SW_MUX_CTL Bits	Configured by SW_MUX_CTL							
			Hardware Mode 1	Hardware Mode 2		Functional Mode	Alternate Mode 1	Alternate Mode 2	Alternate Mode 3	Alternate Mode 4	Alternate Mode 5	Alternate Mode 6	GPIO Mode
NFCLE	EMI	NANDF command latch enable	ATA_DATA 10	ATA_DA0	sw_mux_ctl_nfcle[6:0]	NFC_CLE	—	USBH2_DATA5	—	TRACEDATA_3	—	—	MCU1_13
$\overline{\text{NFWP}}$	EMI	NANDF write protect	ATA_DATA 11	ATA_DA1	sw_mux_ctl_nfwp_b [6:0]	NFC_WP	NFWP_B	USBH2_DATA6	—	TRACEDATA_4	—	—	MCU1_14
$\overline{\text{NFCE}}$	EMI	NANDF chip enable	ATA_DATA 12	ATA_DA2	sw_mux_ctl_nfce_b [6:0]	NFC_CE	—	USBH2_DATA7	—	TRACEDATA_5	—	—	MCU1_15
NFRB	EMI	NANDF ready/busy	ATA_DATA 13	—	sw_mux_ctl_nfrb[6:0]	NFC_RB	—	—	—	TRACEDATA_6	—	—	MCU1_16
D15	EMI	PCMCIA/WEIM/NANDF Data 15	—	—	—	NFC_DATA 15	—	—	—	—	—	—	—
D14	EMI	PCMCIA/WEIM/NANDF Data 14	—	—	—	NFC_DATA 14	—	—	—	—	—	—	—
D13	EMI	PCMCIA/WEIM/NANDF Data 13	—	—	—	NFC_DATA 13	—	—	—	—	—	—	—
D12	EMI	PCMCIA/WEIM/NANDF Data 12	—	—	—	NFC_DATA 12	—	—	—	—	—	—	—
D11	EMI	PCMCIA/WEIM/NANDF Data 11	—	—	—	NFC_DATA 11	—	—	—	—	—	—	—
D10	EMI	PCMCIA/WEIM/NANDF Data 10	—	—	—	NFC_DATA 10	—	—	—	—	—	—	—
D9	EMI	PCMCIA/WEIM/NANDF Data 9	—	—	—	NFC_DATA 9	—	—	—	—	—	—	—
D8	EMI	PCMCIA/WEIM/NANDF Data 8	—	—	—	NFC_DATA 8	—	—	—	—	—	—	—

Table 4-8. Functional Multiplexing Configuration (continued)

Contact Name	Group	Description	Configured by GPR		SW_MUX_CTL Bits	Configured by SW_MUX_CTL							
			Hardware Mode 1	Hardware Mode 2		Functional Mode	Alternate Mode 1	Alternate Mode 2	Alternate Mode 3	Alternate Mode 4	Alternate Mode 5	Alternate Mode 6	GPIO Mode
D7	EMI	PCMCIA/WEIM/NANDF Data 7	—	—	—	NFC_DATA 7	—	—	—	—	—	—	—
D6	EMI	PCMCIA/WEIM/NANDF Data 6	—	—	—	NFC_DATA 6	—	—	—	—	—	—	—
D5	EMI	PCMCIA/WEIM/NANDF Data 5	—	—	—	NFC_DATA 5	—	—	—	—	—	—	—
D4	EMI	PCMCIA/WEIM/NANDF Data 4	—	—	—	NFC_DATA 4	—	—	—	—	—	—	—
D3	EMI	PCMCIA/WEIM/NANDF Data 3	—	—	—	NFC_DATA 3	—	—	—	—	—	—	—
D2	EMI	PCMCIA/WEIM/NANDF Data 2	—	—	—	NFC_DATA 2	—	—	—	—	—	—	—
D1	EMI	PCMCIA/WEIM/NANDF Data 1	—	—	—	NFC_DATA 1	—	—	—	—	—	—	—
D0	EMI	PCMCIA/WEIM/NANDF Data 0	—	—	—	NFC_DATA 0	—	—	—	—	—	—	—
PC_CD1_B	EMI	PCMCIA card detect 1 input	—	—	sw_mux_ctl_pc_cd1_b [6:0]	CD1_B	SD2_CMD	MSHC2_SCLK	—	—	—	—	—
PC_CD2_B	EMI	PCMCIA card detect 2 input	—	—	sw_mux_ctl_pc_cd2_b [6:0]	CD2_B	SD2_CLK	MSHC2_BS	—	—	—	—	—
$\overline{\text{PC\_WAIT}}$	EMI	PCMCIA pending cycle delay input	—	—	sw_mux_ctl_pc_wait_b [6:0]	WAIT_B	SD2_DATA0	MSHC2_SDIO_DATA0	—	—	—	—	—
PC_READY	EMI	PCMCIA ready/busy input	—	—	sw_mux_ctl_pc_ready [6:0]	RDY_IRQ_B	SD2_DATA1	MSHC2_DATA1	—	—	—	—	—

Table 4-8. Functional Multiplexing Configuration (continued)

Contact Name	Group	Description	Configured by GPR		SW_MUX_CTL Bits	Configured by SW_MUX_CTL							
			Hardware Mode 1	Hardware Mode 2		Functional Mode	Alternate Mode 1	Alternate Mode 2	Alternate Mode 3	Alternate Mode 4	Alternate Mode 5	Alternate Mode 6	GPIO Mode
PC_PWRON	EMI	PCMCIA supply ready input	—	—	sw_mux_ctl_pc_pwron [6:0]	PWR_ON	SD2_DATA3	MSHC2_DATA2	—	—	—	—	—
PC_VS1	EMI	PCMCIA voltage sense 1 input	—	—	sw_mux_ctl_pc_vs1 [6:0]	VS1	SD2_DATA2	MSHC2_DATA3	—	—	—	—	—
PC_VS2	EMI	PCMCIA voltage sense 2 input	—	—	sw_mux_ctl_pc_vs2 [6:0]	VS2	USBH2_DATA2	UART5_RTS	—	—	—	—	—
PC_BVD1	EMI	PCMCIA battery voltage detect 1 input	—	—	sw_mux_ctl_pc_bvd1 [6:0]	BVD1	USBH2_DATA3	UART5_RXD	—	—	—	—	—
PC_BVD2	EMI	PCMCIA battery voltage detect 2 input	—	—	sw_mux_ctl_pc_bvd2 [6:0]	BVD2	USBH2_DATA4	UART5_TXD	—	—	—	—	—
PC_RST	EMI	PCMCIA reset output	—	—	sw_mux_ctl_pc_rst [6:0]	CARD_RESET	USBH2_DATA5	UART5_CTS	—	—	—	—	—
IOIS16	EMI	PCMCIA bus width input	—	—	sw_mux_ctl_iois16 [6:0]	IND_WP	USBH2_DATA6	—	—	—	—	—	—
PC_R$\overline{W}$	EMI	PCMCIA read/$\overline{write}$ - external transceiver direction control output.	—	—	sw_mux_ctl_pc_rw_b [6:0]	CARD_RW_B	USBH2_DATA7	—	—	—	—	—	—
PC_POE	EMI	PCMCIA buffers output enable output	—	—	sw_mux_ctl_pc_poe [6:0]	CARD_POE_O_B	—	—	—	—	—	—	—
M_REQUEST	EMI	reserved	—	—	—	M_REQUEST	—	—	—	—	—	—	—

Table 4-8. Functional Multiplexing Configuration (continued)

Contact Name	Group	Description	Configured by GPR		SW_MUX_CTL Bits	Configured by SW_MUX_CTL							
			Hardware Mode 1	Hardware Mode 2		Functional Mode	Alternate Mode 1	Alternate Mode 2	Alternate Mode 3	Alternate Mode 4	Alternate Mode 5	Alternate Mode 6	GPIO Mode
M_GRANT	EMI	reserved	—	—	—	M_GRANT	—	—	—	—	—	—	—
CSI_D4	IPU (CSI)	When using a 10-bit sensor this line is not needed for the sensor data and the suggested use is as the GPIO for IPU CSI chip select1	—	—	sw_mux_ctl_csi_d4 [6:0]	SENSB_DATA[4]	—	—	—	—	—	CTI_TRIG_OUT_1_2	MCU3_4
CSI_D5	IPU (CSI)	When using a 10-bit sensor this line is not needed for the sensor data and the suggested use is as the GPIO for IPU CSI chip select2	—	—	sw_mux_ctl_csi_d5 [6:0]	SENSB_DATA[5]	—	—	—	—	—	CTI_TRIG_OUT_1_3	MCU3_5
CSI_D6	IPU (CSI)	When used with a 10-bit sensor this signal is Sensor Port Data bit 0. If a 16-bit sensor is used it is Sensor Port Data bit 6.	ATA_DATA 0	—	sw_mux_ctl_csi_d6 [6:0]	SENSB_DATA[6]	—	—	—	—	—	CTI_TRIG_OUT_1_4	MCU3_6
CSI_D7	IPU (CSI)	When used with a 10-bit sensor this signal is Sensor Port Data bit 1. If a 16-bit sensor is used it is Sensor Port Data bit 7.	ATA_DATA 1	—	sw_mux_ctl_csi_d7 [6:0]	SENSB_DATA[7]	—	—	—	—	—	CTI_TRIG_OUT_1_5	MCU3_7
CSI_D8	IPU (CSI)	When used with a 10-bit sensor this signal is Sensor Port Data bit 2. If a 16-bit sensor is used it is Sensor Port Data bit 8.	ATA_DATA 2	—	sw_mux_ctl_csi_d8 [6:0]	SENSB_DATA[8]	—	—	—	—	—	—	MCU3_8

Table 4-8. Functional Multiplexing Configuration (continued)

Contact Name	Group	Description	Configured by GPR		SW_MUX_CTL Bits	Configured by SW_MUX_CTL							
			Hardware Mode 1	Hardware Mode 2		Functional Mode	Alternate Mode 1	Alternate Mode 2	Alternate Mode 3	Alternate Mode 4	Alternate Mode 5	Alternate Mode 6	GPIO Mode
CSI_D9	IPU (CSI)	When used with a 10-bit sensor this signal is Sensor Port Data bit 3. If a 16-bit sensor is used it is Sensor Port Data bit 9.	ATA_DATA 3	—	sw_mux_ctl _csi_d9 [6:0]	SENSB_D ATA[9]	—	—	—	—	—	—	MCU3_9
CSI_D10	IPU (CSI)	When used with a 10-bit sensor this signal is Sensor Port Data bit 4. If a 16-bit sensor is used it is Sensor Port Data bit 10.	ATA_DATA 4	—	sw_mux_ctl _csi_d10 [6:0]	SENSB_D ATA[10]	—	—	—	—	—	—	MCU3_ 10
CSI_D11	IPU (CSI)	When used with a 10-bit sensor this signal is Sensor Port Data bit 5. If a 16-bit sensor is used it is Sensor Port Data bit 11.	ATA_DATA 5	—	sw_mux_ctl _csi_d11 [6:0]	SENSB_D ATA[11]	—	—	—	—	—	—	MCU3_ 11
CSI_D12	IPU (CSI)	When used with a 10-bit sensor this signal is Sensor Port Data bit 6. If a 16-bit sensor is used it is Sensor Port Data bit 12.	ATA_DATA 6	—	sw_mux_ctl _csi_d12 [6:0]	SENSB_D ATA[12]	—	—	—	—	—	—	MCU3_ 12
CSI_D13	IPU (CSI)	When used with a 10-bit sensor this signal is Sensor Port Data bit 7. If a 16-bit sensor is used it is Sensor Port Data bit 13.	ATA_DATA 7	—	sw_mux_ctl _csi_d13 [6:0]	SENSB_D ATA[13]	—	—	—	—	—	—	MCU3_ 13

Table 4-8. Functional Multiplexing Configuration (continued)

Contact Name	Group	Description	Configured by GPR		SW_MUX_CTL Bits	Configured by SW_MUX_CTL							
			Hardware Mode 1	Hardware Mode 2		Functional Mode	Alternate Mode 1	Alternate Mode 2	Alternate Mode 3	Alternate Mode 4	Alternate Mode 5	Alternate Mode 6	GPIO Mode
CSI_D14	IPU (CSI)	When used with a 10-bit sensor this signal is Sensor Port Data bit 8. If a 16-bit sensor is used it is Sensor Port Data bit 14.	ATA_DATA 8	—	sw_mux_ctl_csi_d14 [6:0]	SENSB_DATA[14]	—	—	—	—	—	—	MCU3_14
CSI_D15	IPU (CSI)	When used with a 10-bit sensor this signal is Sensor Port Data bit 9. If a 16-bit sensor is used it is Sensor Port Data bit 15.	ATA_DATA 9	—	sw_mux_ctl_csi_d15 [6:0]	SENSB_DATA[15]	—	—	—	—	—	—	MCU3_15
CSI_MCLK	IPU (CSI)	Sensor Port master Clock	ATA_DATA 10	—	sw_mux_ctl_csi_mclk [6:0]	SENSB_MCLK	—	—	—	—	—	—	MCU3_16
CSI_VSYNC	IPU (CSI)	Sensor port vertical sync	ATA_DATA 11	—	sw_mux_ctl_csi_vsync [6:0]	SENSB_VSYNC	—	—	—	—	—	—	MCU3_17
CSI_HSYNC	IPU (CSI)	Sensor port horizontal Sync	ATA_DATA 12	—	sw_mux_ctl_csi_hsync [6:0]	SENSB_HSYNC	—	—	—	—	—	—	MCU3_18
CSI_PIXCLK	IPU (CSI)	Sensor port data latch clock	ATA_DATA 13	—	sw_mux_ctl_csi_pixclk [6:0]	SENSB_PIX_CLK	—	—	—	—	—	—	MCU3_19
I2C_CLK	I2C	I2C clock	ATA_DATA 14	—	sw_mux_ctl_i2c_clk [6:0]	I2C1_SCL	—	—	IPU_DIAGB[0]	—	—	—	—
I2C_DAT	I2C	I2C data	ATA_DATA 15	—	sw_mux_ctl_i2c_dat [6:0]	I2C1_SDA	—	—	IPU_DIAGB[1]	—	—	—	—

Table 4-8. Functional Multiplexing Configuration (continued)

Contact Name	Group	Description	Configured by GPR		SW_MUX_CTL Bits	Configured by SW_MUX_CTL							
			Hardware Mode 1	Hardware Mode 2		Functional Mode	Alternate Mode 1	Alternate Mode 2	Alternate Mode 3	Alternate Mode 4	Alternate Mode 5	Alternate Mode 6	GPIO Mode
STXD3	AudioPort3-BB (HP3)	TxD	ATA_DATA7	USBH2_DATA2	sw_mux_ctl_stxd3[6:0]	HP3_TXDAT	—	—	IPU_DIAGB[2]	TRACEDATA_7	EVNTBUS_0	EMI_DEBUG0	MCU1_17
SRXD3	AudioPort3-BB (HP3)	RxD	ATA_DATA8	USBH2_DATA3	sw_mux_ctl_srxd3[6:0]	HP3_RXDAT	—	—	IPU_DIAGB[3]	TRACEDATA_8	EVNTBUS_1	EMI_DEBUG1	MCU1_18
SCK3	AudioPort3-BB (HP3)	Tx Serial Clock	ATA_DATA9	USBH2_DATA4	sw_mux_ctl_sck3[6:0]	HP3_TXCLK	—	—	IPU_DIAGB[4]	TRACEDATA_9	EVNTBUS_2	EMI_DEBUG2	—
SFS3	AudioPort3-BB (HP3)	Tx Frame Sync	ATA_DATA10	USBH2_DATA5	sw_mux_ctl_sfs3[6:0]	HP3_TXFS	—	—	IPU_DIAGB[5]	TRACEDATA_10	EVNTBUS_3	EMI_DEBUG3	—
STXD4	AudioPort4-PM_NB (PP1)	TxD	—	—	sw_mux_ctl_stxd4[6:0]	PP1_TXDAT	RXFS3	—	IPU_DIAGB[6]	—	EVNTBUS_4	EMI_DEBUG4	MCU1_19
SRXD4	AudioPort4-PM_NB (PP1)	RxD	—	—	sw_mux_ctl_srxd4[6:0]	PP1_RXDAT	RXCLK3	—	IPU_DIAGB[7]	—	EVNTBUS_5	ARM_COREASID0	MCU1_20
SCK4	AudioPort4-PM_NB (PP1)	Tx Serial Clock	—	—	sw_mux_ctl_sck4[6:0]	PP1_TXCLK	RXFS5	—	IPU_DIAGB[8]	—	EVNTBUS_6	ARM_COREASID1	—
SFS4	AudioPort4-PM_NB (PP1)	Tx Frame Sync	—	—	sw_mux_ctl_sfs4[6:0]	PP1_TXFS	RXCLK5	—	IPU_DIAGB[9]	—	EVNTBUS_7	ARM_COREASID2	—

Table 4-8. Functional Multiplexing Configuration (continued)

Contact Name	Group	Description	Configured by GPR		SW_MUX_CTL Bits	Configured by SW_MUX_CTL							
			Hardware Mode 1	Hardware Mode 2		Functional Mode	Alternate Mode 1	Alternate Mode 2	Alternate Mode 3	Alternate Mode 4	Alternate Mode 5	Alternate Mode 6	GPIO Mode
STXD5	AudioPort5-PM_WB (PP2)	TxD	—	—	sw_mux_ctl_stxd5[6:0]	PP2_TXDAT	—	—	IPU_DIAGB[10]	—	EVNTBUS_8	ARM_COREASID3	MCU1_21
SRXD5	AudioPort5-PM_WB (PP2)	RxD	—	—	sw_mux_ctl_srxd5[6:0]	PP2_RXDAT	—	—	IPU_DIAGB[11]	—	EVNTBUS_9	ARM_COREASID4	MCU1_22
SCK5	AudioPort5-PM_WB (PP2)	Tx Serial Clock	—	—	sw_mux_ctl_sck5[6:0]	PP2_TXCLK	—	—	IPU_DIAGB[12]	—	EVNTBUS_10	ARM_COREASID5	—
SFS5	AudioPort5-PM_WB (PP2)	Tx Frame Sync	—	—	sw_mux_ctl_sfs5[6:0]	PP2_TXFS	—	—	IPU_DIAGB[13]	—	EVNTBUS_11	ARM_COREASID6	—
STXD6	AudioPort6-BT (PP3)	TxD	ATA_DATA11	USBH2_DATA6	sw_mux_ctl_stxd6[6:0]	PP3_TXDAT	—	—	IPU_DIAGB[14]	TRACEDATA_11	EVNTBUS_12	ARM_COREASID7	MCU1_23
SRXD6	AudioPort6-BT (PP3)	RxD	ATA_DATA12	USBH2_DATA7	sw_mux_ctl_srxd6[6:0]	PP3_RXDAT	—	—	IPU_DIAGB[15]	TRACEDATA_12	EVNTBUS_13	M3IF_CHOSEN_MASTER_0	MCU1_24
SCK6	AudioPort6-BT (PP3)	Tx Serial Clock	ATA_DATA13	—	sw_mux_ctl_sck6[6:0]	PP3_TXCLK	—	—	IPU_DIAGB[16]	TRACEDATA_13	EVNTBUS_14	M3IF_CHOSEN_MASTER_1	MCU1_25

Table 4-8. Functional Multiplexing Configuration (continued)

Contact Name	Group	Description	Configured by GPR		SW_MUX_CTL Bits	Configured by SW_MUX_CTL							
			Hardware Mode 1	Hardware Mode 2		Functional Mode	Alternate Mode 1	Alternate Mode 2	Alternate Mode 3	Alternate Mode 4	Alternate Mode 5	Alternate Mode 6	GPIO Mode
SFS6	AudioPort6-BT (PP3)	Tx Frame Sync	USBH1_SUSPEND	—	sw_mux_ctl_sfs6[6:0]	PP3_TXFS	—	—	IPU_DIAGB[17]	TRACEDATA_14	EVNTBUS_15	M3IF_CHOSEN_MASTER_2	MCU1_26
CSPI1_MOSI	CSPI1_BB	Master Out/Slave In.	ATA_DATA0	ATA_INTRQ	sw_mux_ctl_cspi1_mosi[6:0]	CSPI1_MOSI	USBH1_RXDM	RXD3	IPU_DIAGB[18]	TRACEDATA_15	—	—	—
CSPI1_MISO	CSPI1_BB	Slave In/Master Out.	ATA_DATA1	ATA_BUFFER_EN	sw_mux_ctl_cspi1_miso[6:0]	CSPI1_MISO	USBH1_RXDP	TXD3	IPU_DIAGB[19]	TRACEDATA_16	—	—	—
CSPI1_SS0	CSPI1_BB	Slave Select (Selectable polarity).	ATA_DATA2	ATA_DMARQ	sw_mux_ctl_cspi1_ss0[6:0]	CSPI1_SS0_B	USBH1_TXDM	CSPI3_SS2	IPU_DIAGB[20]	TRACEDATA_17	—	—	—
CSPI1_SS1	CSPI1_BB	Slave Select (Selectable polarity).	ATA_DATA3	ATA_DA0	sw_mux_ctl_cspi1_ss1[6:0]	CSPI1_SS1_B	USBH1_TXDP	CSPI2_SS3	IPU_DIAGB[21]	TRACEDATA_18	—	—	—
CSPI1_SS2	CSPI1_BB	Slave Select (Selectable polarity).	ATA_DATA4	ATA_DA1	sw_mux_ctl_cspi1_ss2[6:0]	CSPI1_SS2_B	USBH1_RCV	CSPI3_SS3	IPU_DIAGB[22]	TRACEDATA_19	—	—	—
CSPI1_SCLK	CSPI1_BB	Serial Clock.	ATA_DATA5	ATA_DA2	sw_mux_ctl_cspi1_sclk[6:0]	CSPI1_CLK	USBH1_OEB	RTS3	IPU_DIAGB[23]	—	—	—	—
CSPI1_SPI_RDY	CSPI1_BB	Serial Data Ready.	ATA_DATA6	—	sw_mux_ctl_cspi1_spi_rdy[6:0]	CSPI1_IND_DATAREADY_B	USBH1_FS	CTS3	IPU_DIAGB[24]	—	—	—	—
CSPI2_MOSI	CSPI2_PM	Master Out/Slave In.	—	—	sw_mux_ctl_cspi2_mosi[6:0]	CSPI2_MOSI	I2C2_SCL	—	—	—	—	—	—

Table 4-8. Functional Multiplexing Configuration (continued)

Contact Name	Group	Description	Configured by GPR		SW_MUX_CTL Bits	Configured by SW_MUX_CTL							
			Hardware Mode 1	Hardware Mode 2		Functional Mode	Alternate Mode 1	Alternate Mode 2	Alternate Mode 3	Alternate Mode 4	Alternate Mode 5	Alternate Mode 6	GPIO Mode
CSPI2_MISO	CSPI2_PM	Slave In/Master Out.	—	—	sw_mux_ctl_cspi2_miso[6:0]	CSPI2_MISO	I2C2_SDA	—	—	—	—	—	—
CSPI2_SS0	CSPI2_PM	Slave Select (Selectable polarity).	—	—	sw_mux_ctl_cspi2_ss0[6:0]	CSPI2_SS0_B	CSPI3_SS0	—	—	—	—	—	—
CSPI2_SS1	CSPI2_PM	Slave Select (Selectable polarity).	—	—	sw_mux_ctl_cspi2_ss1[6:0]	CSPI2_SS1_B	CSPI3_SS1	CSPI1_SS3	—	—	—	—	—
CSPI2_SS2	CSPI2_PM	Slave Select (Selectable polarity).	—	—	sw_mux_ctl_cspi2_ss2[6:0]	CSPI2_SS2_B	I2C3_SDA	CSI_FLASH_STROBE	—	—	—	—	—
CSPI2_SCLK	CSPI2_PM	Serial Clock.	—	—	sw_mux_ctl_cspi2_sclk[6:0]	CSPI2_CLK	I2C3_SCL	—	—	—	—	—	—
CSPI2_SPI_RDY	CSPI2_PM	—	—	—	sw_mux_ctl_cspi2_spi_rdy[6:0]	CSPI2_DATAREADY_B	—	—	—	—	—	—	—
RXD1	UART1_GPS	Rx Data. (+CE Bus 12)	TRSTB	—	sw_mux_ctl_rxd1[6:0]	UART1_RXD_MUX	USBOTG_DATA4	PP4_TXDAT/STDA	—	DSR_DCE1	—	—	MCU2_4
TXD1	UART1_GPS	Tx Data. + (CE Bus 10)	TCK	—	sw_mux_ctl_txd1[6:0]	UART1_TXD_MUX	USBOTG_DATA1	PP4_TXCLK/SCK	—	RI_DCE1	—	—	MCU2_5
RTS1	UART1_GPS	Request to send. + (CE Bus 9)	—	—	sw_mux_ctl_rts1[6:0]	UART1_RTS_B	—	PP4_TXFS/FS	—	DCD_DCE1	—	—	MCU2_6
CTS1	UART1_GPS	Clear to send. + CE Bus 8)	DE_B	—	sw_mux_ctl_cts1[6:0]	UART1_CTS_B	—	—	—	—	—	—	MCU2_7

Table 4-8. Functional Multiplexing Configuration (continued)

Contact Name	Group	Description	Configured by GPR		SW_MUX_CTL Bits	Configured by SW_MUX_CTL							
			Hardware Mode 1	Hardware Mode 2		Functional Mode	Alternate Mode 1	Alternate Mode 2	Alternate Mode 3	Alternate Mode 4	Alternate Mode 5	Alternate Mode 6	GPIO Mode
DTR_DCE1	UART1_GPS	Full UART IF + CE Bus 11	TMS	—	sw_mux_ctl_dtr_dce1 [6:0]	UART1_DTR_DCE_I_B	—	PP4_RXDAT/SRDA	—	—	—	—	MCU2_8
DSR_DCE1	Full UART IF	Full UART IF + CE Bus 4	TDO	USBOTG_DATA4	sw_mux_ctl_dsr_dce1 [6:0]	UART1_DSR_DCE_O_B	CSPI1_SCLK	TXD1	DSR_DCE2	—	—	—	MCU2_9
RI_DCE1	Full UART IF	Full UART IF + CE Bus 5	TDI	USBOTG_DATA3	sw_mux_ctl_ri_dce1 [6:0]	UART1_RI_DCE_O_B	CSPI1_SPI_RDY	RXD1	RI_DCE2	—	—	—	MCU2_10
DCD_DCE1	Full UART IF	Full UART IF + CE Bus 6	RESET_IN	USBOTG_DATA5	sw_mux_ctl_dcd_dce1 [6:0]	UART1_DCD_DCE_O_B	CSPI1_SS3	RTS1	DCD_DCE2	USB_PWR	—	—	MCU2_11
DTR_DTE1	Full UART IF	—	CSPI1_MOSI	—	sw_mux_ctl_dtr_dte1 [6:0]	UART1_DTR_DTE_O_B	—	—	DTR_DTE2	—	EVNTBUS_16	—	MCU2_12
DSR_DTE1	Full UART IF	—	CSPI1_MISO	—	sw_mux_ctl_dsr_dte1 [6:0]	UART1_DSR_DTE_I_B	DSR_DTE2	—	—	—	EVNTBUS_17	—	MCU2_13
RI_DTE1	Full UART IF	—	CSPI1_SS0	—	sw_mux_ctl_ri_dte1 [6:0]	UART1_RI_DTE_I_B	RI_DTE2	I2C2_SCL	IPU_DIAGB[25]	—	EVNTBUS_18	—	MCU2_14
DCD_DTE1	Full UART IF	—	CSPI1_SS1	—	sw_mux_ctl_dcd_dte1 [6:0]	UART1_DCD_DTE_I_B	DCD_DTE2	I2C2_SDA	IPU_DIAGB[26]	—	EVNTBUS_19	—	MCU2_15
DTR_DCE2	Full UART IF	—	CSPI1_SS2	—	sw_mux_ctl_dtr_dce2 [6:0]	UART2_DTR_DCE_I_B	—	—	IPU_DIAGB[27]	—	—	—	MCU2_16

Table 4-8. Functional Multiplexing Configuration (continued)

Contact Name	Group	Description	Configured by GPR		SW_MUX_CTL Bits	Configured by SW_MUX_CTL							
			Hardware Mode 1	Hardware Mode 2		Functional Mode	Alternate Mode 1	Alternate Mode 2	Alternate Mode 3	Alternate Mode 4	Alternate Mode 5	Alternate Mode 6	GPIO Mode
RXD2	UART2_IR	RX Data	FIRI RXD	—	sw_mux_ctl_rxd2[6:0]	UART2_RXD_MUX	—	—	IPU_DIAGB[28]	—	—	—	MCU1_27
TXD2	UART2_IR	TX Data	FIRI TXD	—	sw_mux_ctl_txd2[6:0]	UART2_TXD_MUX	—	—	IPU_DIAGB[29]	—	—	—	MCU1_28
RTS2	UART2_IR	Request to send	FIRI RXD	—	sw_mux_ctl_rts2[6:0]	UART2_RTS_B	—	—	IPU_DIAGB[30]	—	—	—	—
CTS2	UART2_IR	Clear to send	FIRI TXD	—	sw_mux_ctl_cts2[6:0]	UART2_CTS_B	—	—	IPU_DIAGB[31]	—	—	—	—
BATT_LINE	1-Wire	1-Wire data, external battery monitor	—	—	sw_mux_ctl_batt_line[6:0]	OWIRE_BATTERY_LINE	—	—	—	—	—	—	MCU2_17
KEY_ROW0	Keypad	keypad row sense 0	—	—	sw_mux_ctl_key_row0[6:0]	ROW[0]	—	—	—	—	—	—	—
KEY_ROW1	Keypad	keypad row sense 1	—	—	sw_mux_ctl_key_row1[6:0]	ROW[1]	—	—	—	—	—	—	—
KEY_ROW2	Keypad	keypad row sense 2	—	—	sw_mux_ctl_key_row2[6:0]	ROW[2]	—	—	—	—	—	—	—
KEY_ROW3	Keypad	keypad row sense 3	—	—	sw_mux_ctl_key_row3[6:0]	ROW[3]	—	—	—	TRACECTL	—	—	—
KEY_ROW4	Keypad	keypad row sense 4	—	—	sw_mux_ctl_key_row4[6:0]	ROW[4]	—	—	—	TRACECLK	—	—	MCU2_18

Table 4-8. Functional Multiplexing Configuration (continued)

Contact Name	Group	Description	Configured by GPR		SW_MUX_CTL Bits	Configured by SW_MUX_CTL							
			Hardware Mode 1	Hardware Mode 2		Functional Mode	Alternate Mode 1	Alternate Mode 2	Alternate Mode 3	Alternate Mode 4	Alternate Mode 5	Alternate Mode 6	GPIO Mode
KEY_ROW5	Keypad	keypad row sense 5	—	—	sw_mux_ctl_key_row5 [6:0]	ROW[5]	—	—	—	TRACEDATA_0	—	—	MCU2_19
KEY_ROW6	Keypad	keypad row sense 6	ATA_INTRQ	—	sw_mux_ctl_key_row6 [6:0]	ROW[6]	—	—	—	TRACEDATA_1	—	—	MCU2_20
KEY_ROW7	Keypad	keypad row sense 7	ATA_BUFFER_EN	—	sw_mux_ctl_key_row7 [6:0]	ROW[7]	—	—	—	TRACEDATA_2	—	—	MCU2_21
KEY_COL0	Keypad	keypad column driver 0	—	—	sw_mux_ctl_key_col0 [6:0]	COL[0]	—	—	—	—	—	—	—
KEY_COL1	Keypad	keypad column driver 1	—	—	sw_mux_ctl_key_col1 [6:0]	COL[1]	—	—	—	—	—	—	—
KEY_COL2	Keypad	keypad column driver 2	—	—	sw_mux_ctl_key_col2 [6:0]	COL[2]	—	—	—	—	—	—	—
KEY_COL3	Keypad	keypad column driver 3	—	—	sw_mux_ctl_key_col3 [6:0]	COL[3]	—	—	—	TRACEDATA_3	—	—	—
KEY_COL4	Keypad	keypad column driver 4	ATA_DMARQ	—	sw_mux_ctl_key_col4 [6:0]	COL[4]	—	—	—	TRACEDATA_4	—	—	MCU2_22
KEY_COL5	Keypad	keypad column driver 5	ATA_DA0	—	sw_mux_ctl_key_col5 [6:0]	COL[5]	—	—	—	TRACEDATA_5	—	—	MCU2_23
KEY_COL6	Keypad	keypad column driver 6	ATA_DA1	—	sw_mux_ctl_key_col6 [6:0]	COL[6]	—	—	—	TRACEDATA_6	—	—	MCU2_24

Table 4-8. Functional Multiplexing Configuration (continued)

Contact Name	Group	Description	Configured by GPR		SW_MUX_CTL Bits	Configured by SW_MUX_CTL							
			Hardware Mode 1	Hardware Mode 2		Functional Mode	Alternate Mode 1	Alternate Mode 2	Alternate Mode 3	Alternate Mode 4	Alternate Mode 5	Alternate Mode 6	GPIO Mode
KEY_COL7	Keypad	keypad column driver 7	ATA_DA2	—	sw_mux_ctl_key_col7 [6:0]	COL[7]	—	—	—	TRACEDATA_7	—	—	MCU2_25
RTCK	JTAG	ARM debug test clock	—	—	—	DBGRTCK	—	—	—	—	—	—	—
TCK	JTAG	JTAG Tap clock	—	—	sw_mux_ctl_tck[6:0]	TCK	—	—	—	—	—	—	—
TMS	JTAG	JTAG Tap mode select	—	—	sw_mux_ctl_tms[6:0]	TMS	—	—	—	—	—	—	—
TDI	JTAG	JTAG Tap Data In	—	—	sw_mux_ctl_tdi[6:0]	TDI	—	—	—	—	—	—	—
TDO	JTAG	JTAG Tap data out	—	—	—	TDO	—	—	—	—	—	—	—
TRSTB	JTAG	JTAG Tap reset	—	—	sw_mux_ctl_trstb[6:0]	TRST_B	—	—	—	—	—	—	—
DE_B	JTAG	JTAG debug enable	—	—	sw_mux_ctl_de_b[6:0]	DEBUG_IN_B	—	—	—	—	—	—	—
SJC_MOD	JTAG	JTAG Mode	—	—	—	SJC_MOD	—	—	—	—	—	—	—
USB_PWR	USB GEN	USB Generic	—	—	sw_mux_ctl_usb_pwr [6:0]	USB_PWR	—	—	—	—	—	MAX1_HMASTER_0	MCU1_29
USB_OC	USB GEN	USB Generic	—	—	sw_mux_ctl_usb_oc [6:0]	USB_OC	—	—	—	—	—	MAX1_HMASTER_1	MCU1_30
USB_BYP	USB GEN	USB Generic	—	—	sw_mux_ctl_usb_byp [6:0]	USB_BYPASS_B	—	—	—	—	—	MAX1_HMASTER_2	MCU1_31

Table 4-8. Functional Multiplexing Configuration (continued)

Contact Name	Group	Description	Configured by GPR		SW_MUX_CTL Bits	Configured by SW_MUX_CTL							
			Hardware Mode 1	Hardware Mode 2		Functional Mode	Alternate Mode 1	Alternate Mode 2	Alternate Mode 3	Alternate Mode 4	Alternate Mode 5	Alternate Mode 6	GPIO Mode
USBOTG_CLK	USBOTG	USB OTG FS/ULPI Port	—	—	sw_mux_ctl_usbotg_clk[6:0]	OTG_CLK	—	—	—	—	—	MAX1_HMASTER_3	—
USBOTG_DIR	USBOTG	USB OTG FS/ULPI Port	—	—	sw_mux_ctl_usbotg_dir[6:0]	OTG_DIR	—	—	—	—	—	MAX0_HMASTER_0	—
USBOTG_STP	USBOTG	USB OTG FS/ULPI Port	—	—	sw_mux_ctl_usbotg_stp[6:0]	OTG_STP	—	—	—	—	—	MAX0_HMASTER_1	—
USBOTG_NXT	USBOTG	USB OTG FS/ULPI Port	—	—	sw_mux_ctl_usbotg_nxt[6:0]	OTG_NXT	—	—	—	—	—	MAX0_HMASTER_2	—
USBOTG_DATA0	USBOTG	USB OTG FS/ULPI Port + CE Bus	—	—	sw_mux_ctl_usbotg_data0[6:0]	OTG_DATA0	—	UART4_CTS	—	—	—	MAX0_HMASTER_3	—
USBOTG_DATA1	USBOTG	USB OTG FS/ULPI Port	—	—	sw_mux_ctl_usbotg_data1[6:0]	OTG_DATA1	—	—	—	—	—	—	—
USBOTG_DATA2	USBOTG	USB OTG FS/ULPI Port + CE Bus	—	—	sw_mux_ctl_usbotg_data2[6:0]	OTG_DATA2	—	—	—	—	—	—	—
USBOTG_DATA3	USBOTG	USB OTG FS/ULPI Port	—	—	sw_mux_ctl_usbotg_data3[6:0]	OTG_DATA3	—	UART4_RXD	—	—	—	—	—

Table 4-8. Functional Multiplexing Configuration (continued)

Contact Name	Group	Description	Configured by GPR		SW_MUX_CTL Bits	Configured by SW_MUX_CTL							
			Hardware Mode 1	Hardware Mode 2		Functional Mode	Alternate Mode 1	Alternate Mode 2	Alternate Mode 3	Alternate Mode 4	Alternate Mode 5	Alternate Mode 6	GPIO Mode
USBOTG_DATA4	USBOTG	USB OTG FS/ULPI Port	—	—	sw_mux_ctl_usbotg_data4[6:0]	OTG_DATA4	—	UART4_TXD	—	—	—	—	—
USBOTG_DATA5	USBOTG	USB OTG FS/ULPI Port	—	—	sw_mux_ctl_usbotg_data5[6:0]	OTG_DATA5	—	UART4_RTS	—	—	—	—	—
USBOTG_DATA6	USBOTG	USB OTG FS/ULPI Port	—	—	sw_mux_ctl_usbotg_data6[6:0]	OTG_DATA6	—	—	—	—	—	—	—
USBOTG_DATA7	USBOTG	USB OTG FS/ULPI Port	—	—	sw_mux_ctl_usbotg_data7[6:0]	OTG_DATA7	—	—	—	—	—	—	—
USBH2_CLK	USBH2	USB Host2 FS/ULPI	ATA_INTRQ	—	sw_mux_ctl_usbh2_clk[6:0]	UH2_CLK	UART5_RTS	—	—	TRACEDATA_20	—	—	—
USBH2_DIR	USBH2	USB Host2 FS/ULPI	ATA_BUFFER_EN	—	sw_mux_ctl_usbh2_dir[6:0]	UH2_DIR	UART5_RXD	—	—	TRACEDATA_21	—	—	—
USBH2_STP	USBH2	USB Host2 FS/ULPI	ATA_DMARQ	—	sw_mux_ctl_usbh2_stp[6:0]	UH2_STP	UART5_TXD	—	—	TRACEDATA_22	—	—	—
USBH2_NXT	USBH2	USB Host2 FS/ULPI	ATA_DA0	—	sw_mux_ctl_usbh2_nxt[6:0]	UH2_NXT	UART5_CTS	—	—	TRACEDATA_23	—	—	—
USBH2_DATA0	USBH2	USB Host2 FS/ULPI	ATA_DA1	—	sw_mux_ctl_usbh2_data0[6:0]	UH2_DATA0	—	—	—	TRACECTL	—	—	—
USBH2_DATA1	USBH2	USB Host2 FS/ULPI	ATA_DA2	—	sw_mux_ctl_usbh2_data1[6:0]	UH2_DATA1	—	—	—	TRACECLK	—	—	—

Table 4-8. Functional Multiplexing Configuration (continued)

Contact Name	Group	Description	Configured by GPR		SW_MUX_CTL Bits	Configured by SW_MUX_CTL							
			Hardware Mode 1	Hardware Mode 2		Functional Mode	Alternate Mode 1	Alternate Mode 2	Alternate Mode 3	Alternate Mode 4	Alternate Mode 5	Alternate Mode 6	GPIO Mode
LD0	IPU (LCD)	—	—	—	sw_mux_ctl_ld0[6:0]	DISPB_DATA[0]	—	—	—	—	—	SDMA_DEBUG_PC_0	—
LD1	IPU (LCD)	—	—	—	sw_mux_ctl_ld1[6:0]	DISPB_DATA[1]	—	—	—	—	—	SDMA_DEBUG_PC_1	—
LD2	IPU (LCD)	—	—	—	sw_mux_ctl_ld2[6:0]	DISPB_DATA[2]	—	—	—	—	—	SDMA_DEBUG_PC_2	—
LD3	IPU (LCD)	—	—	—	sw_mux_ctl_ld3[6:0]	DISPB_DATA[3]	—	—	—	—	—	SDMA_DEBUG_PC_3	—
LD4	IPU (LCD)	—	—	—	sw_mux_ctl_ld4[6:0]	DISPB_DATA[4]	—	—	—	—	—	SDMA_DEBUG_PC_4	—
LD5	IPU (LCD)	—	—	—	sw_mux_ctl_ld5[6:0]	DISPB_DATA[5]	—	—	—	—	—	SDMA_DEBUG_PC_5	—
LD6	IPU (LCD)	—	—	—	sw_mux_ctl_ld6[6:0]	DISPB_DATA[6]	—	—	—	—	—	SDMA_DEBUG_PC_6	—

Table 4-8. Functional Multiplexing Configuration (continued)

Contact Name	Group	Description	Configured by GPR		SW_MUX_CTL Bits	Configured by SW_MUX_CTL							
			Hardware Mode 1	Hardware Mode 2		Functional Mode	Alternate Mode 1	Alternate Mode 2	Alternate Mode 3	Alternate Mode 4	Alternate Mode 5	Alternate Mode 6	GPIO Mode
LD7	IPU (LCD)	—	—	—	sw_mux_ctl_ld7[6:0]	DISPB_DATA[7]	—	—	—	—	—	SDMA_DEBUG_PC_7	—
LD8	IPU (LCD)	—	—	—	sw_mux_ctl_ld8[6:0]	DISPB_DATA[8]	—	—	—	—	—	SDMA_DEBUG_PC_8	—
LD9	IPU (LCD)	—	—	—	sw_mux_ctl_ld9[6:0]	DISPB_DATA[9]	—	—	—	—	—	SDMA_DEBUG_PC_9	—
LD10	IPU (LCD)	—	—	—	sw_mux_ctl_ld10[6:0]	DISPB_DATA[10]	—	—	—	—	—	SDMA_DEBUG_PC_10	—
LD11	IPU (LCD)	—	—	—	sw_mux_ctl_ld11[6:0]	DISPB_DATA[11]	—	—	—	—	—	SDMA_DEBUG_PC_11	—
LD12	IPU (LCD)	—	—	—	sw_mux_ctl_ld12[6:0]	DISPB_DATA[12]	—	—	—	—	—	SDMA_DEBUG_PC_12	—
LD13	IPU (LCD)	—	—	—	sw_mux_ctl_ld13[6:0]	DISPB_DATA[13]	—	—	—	—	—	SDMA_DEBUG_PC_13	—

Table 4-8. Functional Multiplexing Configuration (continued)

Contact Name	Group	Description	Configured by GPR		SW_MUX_CTL Bits	Configured by SW_MUX_CTL							
			Hardware Mode 1	Hardware Mode 2		Functional Mode	Alternate Mode 1	Alternate Mode 2	Alternate Mode 3	Alternate Mode 4	Alternate Mode 5	Alternate Mode 6	GPIO Mode
LD14	IPU (LCD)	—	—	—	sw_mux_ctl_ld14[6:0]	DISPB_DATA[14]	—	—	—	—	—	SDMA_DEBUG_EVENT_CHANNEL_0	—
LD15	IPU (LCD)	—	—	—	sw_mux_ctl_ld15[6:0]	DISPB_DATA[15]	—	—	—	—	—	SDMA_DEBUG_EVENT_CHANNEL_1	—
LD16	IPU (LCD)	—	—	—	sw_mux_ctl_ld16[6:0]	DISPB_DATA[16]	—	—	—	—	—	SDMA_DEBUG_EVENT_CHANNEL_2	—
LD17	IPU (LCD)	—	—	—	sw_mux_ctl_ld17[6:0]	DISPB_DATA[17]	—	—	—	—	—	SDMA_DEBUG_EVENT_CHANNEL_3	—

Table 4-8. Functional Multiplexing Configuration (continued)

Contact Name	Group	Description	Configured by GPR		SW_MUX_ CTL Bits	Configured by SW_MUX_CTL							
			Hardware Mode 1	Hardware Mode 2		Functional Mode	Alternate Mode 1	Alternate Mode 2	Alternate Mode 3	Alternate Mode 4	Alternate Mode 5	Alternate Mode 6	GPIO Mode
VSYNC0	IPU (LCD)	frame sync	—	—	sw_mux_ctl _vsync0 [6:0]	DISPB_D0 _VSYNC	—	—	—	—	—	SDM A_DE BUG_ EVEN T_CH ANNE L_4	—
HSYNC	IPU (LCD)	line sync	—	—	sw_mux_ctl _hsync[6:0]	DISPB_D3 _HSYNC	—	—	—	—	—	SDM A_DE BUG_ EVEN T_CH ANNE L_5	—
FPSHIFT	IPU (LCD)	shift	—	—	sw_mux_ctl _fpshift[6:0]	DISPB_D3 _CLK	DISP B_BC LK	—	—	—	—	SDM A_DE BUG_ COR E_ST ATUS _0	—
DRDY0	IPU (LCD)	DRDY/VLD	—	—	sw_mux_ctl _drdy0[6:0]	DISPB_D3 _DRDY	—	—	—	—	—	SDM A_DE BUG_ COR E_ST ATUS _1	—

Table 4-8. Functional Multiplexing Configuration (continued)

Contact Name	Group	Description	Configured by GPR		SW_MUX_CTL Bits	Configured by SW_MUX_CTL							
			Hardware Mode 1	Hardware Mode 2		Functional Mode	Alternate Mode 1	Alternate Mode 2	Alternate Mode 3	Alternate Mode 4	Alternate Mode 5	Alternate Mode 6	GPIO Mode
SD_D_I	IPU (LCD)	Data in for Serial Display	—	—	sw_mux_ctl_sd_d_i[6:0]	—	—	SD_D_I	—	—	—	SDMA_DEBUG_CORE_STATUS_2	MCU3_20
SD_D_IO	IPU (LCD)	Data in/out for Serial Display	—	—	sw_mux_ctl_sd_d_io [6:0]	DISPB_SD_D	—	—	—	—	—	SDMA_DEBUG_CORE_STATUS_3	MCU3_21
SD_D_CLK	IPU (LCD)	Serial Display clock	—	—	sw_mux_ctl_sd_d_clk [6:0]	DISPB_SD_D_CLK	—	—	—	—	—	—	MCU3_22
LCS0	IPU (LCD)	Asynch. Port chip select	—	—	sw_mux_ctl_lcs0[6:0]	DISPB_D0_CS	DISPB_BCLK	—	—	—	—	—	MCU3_23
LCS1	IPU (LCD)	Asynch. Port chip select	—	—	sw_mux_ctl_lcs1[6:0]	DISPB_D1_C	—	—	—	—	—	—	MCU3_24
SER_RS	IPU (LCD)	Asynch. Serial Port data/comm	—	—	sw_mux_ctl_ser_rs [6:0]	DISPB_SER_RS	—	—	—	—	—	—	MCU3_25
PAR_RS	IPU (LCD)	Asynch.Parallel Port data/comm	—	—	sw_mux_ctl_par_rs [6:0]	DISPB_PAR_RS	—	—	—	—	—	—	—
WRITE	IPU (LCD)	Asynch. Port write	—	—	sw_mux_ctl_write[6:0]	DISPB_WR	—	—	—	—	—	—	—

Table 4-8. Functional Multiplexing Configuration (continued)

Contact Name	Group	Description	Configured by GPR		SW_MUX_CTL Bits	Configured by SW_MUX_CTL							
			Hardware Mode 1	Hardware Mode 2		Functional Mode	Alternate Mode 1	Alternate Mode 2	Alternate Mode 3	Alternate Mode 4	Alternate Mode 5	Alternate Mode 6	GPIO Mode
READ	IPU (LCD)	Asynch. Port read	—	—	sw_mux_ctl_read[6:0]	DISPB_RD	—	—	—	—	—	—	—
VSYNC3	IPU (LCD)	vsync	—	—	sw_mux_ctl_vsync3 [6:0]	DISPB_D3_VSYNC	—	—	—	—	—	—	—
CONTRAST	IPU (LCD)	—	—	—	sw_mux_ctl_contrast [6:0]	DISPB_CONTRAST	—	—	—	—	—	—	—
D3_REV	IPU (LCD)	—	—	—	sw_mux_ctl_d3_rev [6:0]	DISPB_D3_REV	—	—	—	—	—	—	—
D3_CLS	IPU (LCD)	—	—	—	sw_mux_ctl_d3_cls [6:0]	DISPB_D3_CLS	—	—	—	—	—	—	—
D3_SPL	IPU (LCD)	—	—	—	sw_mux_ctl_d3_spl [6:0]	DISPB_D3_SPL	—	—	—	—	—	—	—
SD1_CMD	SD/MMC 1	—	—	—	sw_mux_ctl_sd1_cmd [6:0]	SDHC1_CMD	MSHC1_SCLK	—	—	TRACEDATA_0	—	—	MCU2_26
SD1_CLK	SD/MMC 1	—	—	—	sw_mux_ctl_sd1_clk [6:0]	SDHC1_MMC_CLK	MSHC1_BS	—	—	TRACEDATA_1	—	—	MCU2_27
SD1_DATA0	SD/MMC 1	—	—	—	sw_mux_ctl_sd1_data0[6:0]	SDHC1_DATA0	MSHC1_SDIO_DATA0	—	—	TRACEDATA_2	—	—	MCU2_28

Table 4-8. Functional Multiplexing Configuration (continued)

Contact Name	Group	Description	Configured by GPR		SW_MUX_CTL Bits	Configured by SW_MUX_CTL							
			Hardware Mode 1	Hardware Mode 2		Functional Mode	Alternate Mode 1	Alternate Mode 2	Alternate Mode 3	Alternate Mode 4	Alternate Mode 5	Alternate Mode 6	GPIO Mode
SD1_DATA1	SD/MMC 1	—	—	—	sw_mux_ctl_sd1_data1[6:0]	SDHC1_DATA1	MSHC1_DATA1	—	—	TRACEDATA_3	—	—	MCU2_29
SD1_DATA2	SD/MMC 1	—	—	—	sw_mux_ctl_sd1_data2[6:0]	SDHC1_DATA2	MSHC1_DATA2	—	—	TRACEDATA_4	—	—	MCU2_30
SD1_DATA3	SD/MMC 1	—	—	—	sw_mux_ctl_sd1_data3[6:0]	SDHC1_DATA3	MSHC1_DATA3	CTI_TRIG_IN_1_7	—	TRACEDATA_5	—	—	MCU2_31
ATA_CS0	ATA	—	—	—	sw_mux_ctl_ata_cs0[6:0]	ATA_CS0	UART4_RXD	CSI_D0	SD_D_CLK	TRACEDATA_6	—	—	MCU3_26
ATA_CS1	ATA	—	—	—	sw_mux_ctl_ata_cs1[6:0]	ATA_CS1	UART4_RTS	CSI_D1	LCS1	TRACEDATA_7	—	—	MCU3_27
ATA_DIOR	ATA	—	—	—	sw_mux_ctl_ata_dior[6:0]	ATA_DIOR	UART4_TXD	CSI_D2	SER_RS	TRACECTL	—	—	MCU3_28
ATA_DIOW	ATA	—	—	—	sw_mux_ctl_ata_diow[6:0]	ATA_DIOW	UART4_CTS	CSI_D3	—	TRACECLK	—	—	MCU3_29
ATA_DMACK	ATA	—	—	—	sw_mux_ctl_ata_dmack[6:0]	ATA_DMACK	SD_D_O	—	—	—	—	—	MCU3_30
ATA_RESET_B	ATA	—	—	—	sw_mux_ctl_ata_reset_b[6:0]	ATA_RESET_B	SD_D	—	—	—	—	—	MCU3_31
CE_CONTROL	CE CONTROL	—	—	—	—	CE_CONTROL	—	—	—	—	—	—	—

Table 4-8. Functional Multiplexing Configuration (continued)

Contact Name	Group	Description	Configured by GPR		SW_MUX_CTL Bits	Configured by SW_MUX_CTL							
			Hardware Mode 1	Hardware Mode 2		Functional Mode	Alternate Mode 1	Alternate Mode 2	Alternate Mode 3	Alternate Mode 4	Alternate Mode 5	Alternate Mode 6	GPIO Mode
CLKSS	Clock and Reset and PM	Clock Source Select at reset	—	—	—	CLKSS	—	—	—	—	—	—	—
CSPI3_MOSI	CSPI3_MM	Master Out/Slave In	—	—	sw_mux_ctl_cspi3_mosi[6:0]	CSPI3_MOSI	RXD3	—	—	—	—	—	—
CSPI3_MISO	CSPI3_MM	Slave In/Master Out	—	—	sw_mux_ctl_cspi3_miso[6:0]	CSPI3_MISO	TXD3	—	—	—	—	—	—
CSPI3_SCLK	CSPI3_MM	Serial Clock	—	—	sw_mux_ctl_cspi3_sclk[6:0]	CSPI3_CLK	RTS3	—	—	—	—	—	—
CSPI3_SPI_RDY	CSPI3_MM	Serial Data Ready	—	—	sw_mux_ctl_cspi3_spi_rdy[6:0]	CSPI3_IND_DATAREADY_B	CTS3	—	—	—	—	—	—
TTM_PAD	TTM_PAD	Special TTM pad, factory use only.	—	—	—	—	—	—	—	—	—	—	—

4.3.6 ATA Routing Options

Table 4-9 lists seven signal routing options for the ATA signals. The primary purpose of this table is to provide a summary of the seven most commonly used routing scenarios of the ATA signals that are controlled by the hardware modes.

Table 4-9. ATA Signal Routing Options using Hardware Modes

Group	Scenario A Mux Mode; GPR Bit; ATA Signals	Scenario B Mux Mode; GPR Bit; ATA Signals	Scenario C Mux Mode; GPR Bit; ATA Signals	Scenario D Mux Mode; GPR Bit; ATA Signals	Scenario E Mux Mode; GPR Bit; ATA Signals	Scenario F Mux Mode; GPR Bit; ATA Signals	Scenario G Mux Mode; GPR Bit; ATA Signals
PWM	HW1; GPR[3]; IORDY	HW1; GPR[3]; IORDY	HW1; GPR[3]; IORDY	HW1; GPR[3]; IORDY	HW1; GPR[3]; IORDY	HW1; GPR[3]; IORDY	HW1; GPR[3]; IORDY
Timer	HW1; GPR[9]; DATA[14,15]	HW1; GPR[9]; DATA[14,15]	–	–	–	HW1; GPR[9]; DATA[14,15]	HW1; GPR[9]; DATA[14,15]
EMI (NANDFC)	HW1; GPR[5]; DATA[7:13]	–	–	–	HW2; GPR[6]; DA0-2, DMARQ, INTRQ, BUFFER_EN	HW2; GPR[6]; DA0-2, DMARQ, INTRQ, BUFFER_EN	–
IPU (CSI)	–	–	HW1; GPR[7]; DATA[0:13]	HW1; GPR[7]; DATA[0:13]	HW1; GPR[7]; DATA[0:13]	–	–
AudioPort3	–	HW1; GPR[8]; DATA[7:10]	–	–	–	HW1; GPR[8]; DATA[7:10]	HW1; GPR[8]; DATA[7:10]
AudioPort6	–	HW1; GPR[8]; DATA[11:13]	–	–	–	HW1; GPR[8]; DATA[11:13]	HW1; GPR[8]; DATA[11:13]
Keypad	–	HW1; GPR[26]; DA0-2, DMARQ, INTRQ, BUFFER_EN	–	–	–	–	–
CSPI1	HW1; GPR[9]; DATA[0:6]	HW1; GPR[9]; DATA[0:6]	–	HW2; GPR[10]; DA0-2, DMARQ, INTRQ, BUFFER_EN	–	HW1; GPR[9]; DATA[0:6]	HW1; GPR[9]; DATA[0:6]
USBH2	HW1; GPR[4]; DA0-2, DMARQ, INTRQ, BUFFER_EN	–	HW1; GPR[4]; DA0-2, DMARQ, INTRQ, BUFFER_EN	–	–	–	HW1; GPR[4]; DA0-2, DMARQ, INTRQ, BUFFER_EN

Table 4-9. ATA Signal Routing Options using Hardware Modes (continued)

Group	Scenario A Mux Mode; GPR Bit; ATA Signals	Scenario B Mux Mode; GPR Bit; ATA Signals	Scenario C Mux Mode; GPR Bit; ATA Signals	Scenario D Mux Mode; GPR Bit; ATA Signals	Scenario E Mux Mode; GPR Bit; ATA Signals	Scenario F Mux Mode; GPR Bit; ATA Signals	Scenario G Mux Mode; GPR Bit; ATA Signals
I2C	–	–	HW1; GPR[7]; DATA[14,15]	HW1; GPR[7]; DATA[14,15]	HW1; GPR[7]; DATA[14,15]	–	–
ATA	Functional; (no GPR bit); DIOR, DIOW, CS0, CS1, RESET_B, DMACK	Functional; (no GPR bit); DIOR, DIOW, CS0, CS1, RESET_B, DMACK	Functional; (no GPR bit); DIOR, DIOW, CS0, CS1, RESET_B, DMACK	Functional; (no GPR bit); DIOR, DIOW, CS0, CS1, RESET_B, DMACK	Functional; (no GPR bit); DIOR, DIOW, CS0, CS1, RESET_B, DMACK	Functional; (no GPR bit); DIOR, DIOW, CS0, CS1, RESET_B, DMACK	Functional; (no GPR bit); DIOR, DIOW, CS0, CS1, RESET_B, DMACK

See Table 4-8 for (Contact) Group, (Functional) Mux Modes, and associated Contact Signal list. See Table 4-5 for GPR bit and Mux Mode information. A dash indicates that a Contact Group is not used for a particular Scenario. Therefore, the Group may be used for other signal multiplexing.

4.3.7 Software Pad Control Register (SW_PAD_CTL)

The SW_PAD_CTL registers control the characteristics of the I/O lines. Figure 4-88 provides the register's field descriptions; Table 4-10 lists the control by bit.

0x43FA_C154
to
0x43FA_C308

Access: User Read/Write

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R			SW_PAD_CTL_IO3										SW_PAD_CTL_IO2			
W			loopback	ipp_pke	ipp_pue	ipp_pus0	ipp_pus1	ipp_hys	ipp_ode	ipp_dse1	ipp_dse0	ipp_sre	loopback	ipp_pke	ipp_pue	ipp_pus0
Field bits	—	—	9	8	7	6	5	4	3	2	1	0	9	8	7	6

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	SW_PAD_CTL_IO2						SW_PAD_CTL_IO1									
W	ipp_pus1	ipp_hys	ipp_ode	ipp_dse1	ipp_dse0	ipp_sre	loopback	ipp_pke	ipp_pue	ipp_pus0	ipp_pus1	ipp_hys	ipp_ode	ipp_dse1	ipp_dse0	ipp_sre
Field bits	5	4	3	2	1	0	9	8	7	6	5	4	3	2	1	0

Figure 4-88. SW_PAD_CTL

Table 4-10. SW_PAD_CTL Bit Descriptions

Register Bit	Bit Name	Description
SW_PAD_CTL[31:30]	—	Unused
SW_PAD_CTL[29] SW_PAD_CTL[19] SW_PAD_CTL[9]	Loopback	Used to loop back the logic level at the BGA ball to a module input. Used when programming an output value to verify the value is achieved at I/O 0 Disable 1 Enable
SW_PAD_CTL[28:27] SW_PAD_CTL[18:17] SW_PAD_CTL[8:7]	ipp_pke ipp_pue	Pull-up, pull-down, and keeper 00 Disable pull-up/down, and keeper 01 Disable pull-up/down, and keeper 10 Enable keeper 11 Enable pull-up or pull-down
SW_PAD_CTL[26:25] SW_PAD_CTL[16:15] SW_PAD_CTL[6:5]	ipp_pus0 ipp_pus1	Size of pull resistor and up/down control 00 100 kΩ pull-down 01 100 kΩ pull-up 10 47 kΩ pull-up (Not used in i.MX31 and i.MX31L.) 11 22 kΩ pull-up (Not used in i.MX31 and i.MX31L.)
SW_PAD_CTL[24] SW_PAD_CTL[14] SW_PAD_CTL[4]	ipp_hys	Hysteresis control 0 Standard input 1 Input with hysteresis, Schmitt trigger engaged
SW_PAD_CTL[23] SW_PAD_CTL[13] SW_PAD_CTL[3]	ipp_ode	Open-drain control 0 Standard CMOS output, push-pull 1 Output is open-drain (requires pull-up)
SW_PAD_CTL[22:21] SW_PAD_CTL[12:11] SW_PAD_CTL[2:1]	ipp_dse1 ipp_dse0	Output drive strength 00 Standard (std) 01 High 10 Max 11 Max
SW_PAD_CTL[20] SW_PAD_CTL[10] SW_PAD_CTL[0]	ipp_sre	Slew rate control 0 Slow 1 Fast

4.3.8 Register Descriptions for SW Pad Control (SW_PAD_CTL)

Figure 4-89 through Figure 4-198 show the sw_pad_ctl registers. The I/O settings shown in Table 4-12 enables the user to select the characteristics of each I/O line by configuring the appropriate SW_PAD_CTL registers.

Absolute: 0x43FA_C154 Access: User Read/Write

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R			sw_pad_ctl_ttm_pad										Reserved			
W																
Reset	0	0	0	0	1	0	1	0	0	0	0	0	0	0	0	0

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	Reserved						Reserved									
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Figure 4-89. Register Description sw_pad_ctl_ttm_pad__x__x

Absolute: 0x43FA_C158 Access: User Read/Write

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R			sw_pad_ctl_cspi3_miso										sw_pad_ctl_cspi3_sclk			
W																
Reset	0	0	0	1	1	0	1	0	0	0	0	0	0	1	1	0

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	sw_pad_ctl_cspi3_sclk						sw_pad_ctl_cspi3_spi_rdy									
W																
Reset	1	1	0	0	0	0	0	1	1	0	1	0	0	0	0	0

Figure 4-90. Register Description sw_pad_ctl_cspi3_miso_cspi3_sclk_cspi3_spi_rdy

Absolute: 0x43FA_C15C Access: User Read/Write

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R			sw_pad_ctl_ce_control										sw_pad_ctl_clkss			
W																
Reset	0	0	0	0	1	0	0	0	0	0	0	1	0	0	1	0

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	sw_pad_ctl_clkss						sw_pad_ctl_cspi3_mosi									
W																
Reset	1	0	0	0	0	1	0	1	1	0	1	0	0	0	0	0

Figure 4-91. Register Description sw_pad_ctl_ce_control_clkss_cspi3_mosi

Absolute: 0x43FA_C160 Access: User Read/Write

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R			sw_pad_ctl_ata_diow										sw_pad_ctl_ata_dmack			
W																
Reset	0	0	0	1	1	0	1	0	0	0	0	0	0	1	1	0

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	sw_pad_ctl_ata_dmack						sw_pad_ctl_ata_reset_b									
W																
Reset	1	0	0	0	0	0	0	1	1	0	1	0	0	0	0	0

Figure 4-92. Register Description sw_pad_ctl_ata_diow_ata_dmack_ata_reset_b

Absolute: 0x43FA_C164 Access: User Read/Write

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R			sw_pad_ctl_ata_cs0										sw_pad_ctl_ata_cs1			
W																
Reset	0	0	0	0	1	0	1	0	0	0	0	0	0	0	1	0

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	sw_pad_ctl_ata_cs1						sw_pad_ctl_ata_dior									
W																
Reset	1	0	0	0	0	0	0	1	1	0	1	0	0	0	0	0

Figure 4-93. Register Description sw_pad_ctl_ata_cs0_ata_cs1_ata_dior

Absolute: 0x43FA_C168 Access: User Read/Write

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R			sw_pad_ctl_sd1_data1										sw_pad_ctl_sd1_data2			
W																
Reset	0	0	0	0	1	0	1	0	0	0	0	1	0	0	1	0

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	sw_pad_ctl_sd1_data2						sw_pad_ctl_sd1_data3									
W																
Reset	1	0	0	0	0	1	0	0	1	0	0	0	0	0	0	1

Figure 4-94. Register Description sw_pad_ctl_sd1_data1_sd1_data2_sd1_data3

Absolute: 0x43FA_C16C Access: User Read/Write

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R			sw_pad_ctl_sd1_cmd										sw_pad_ctl_sd1_clk			
W																
Reset	0	0	0	0	1	0	1	0	0	0	0	1	0	0	1	0

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	sw_pad_ctl_sd1_clk						sw_pad_ctl_sd1_data0									
W																
Reset	1	0	0	0	0	1	0	0	1	0	1	0	0	0	0	1

Figure 4-95. Register Description sw_pad_ctl_sd1_cmd_sd1_clk_sd1_data0

Absolute: 0x43FA_C170 Access: User Read/Write

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R			sw_pad_ctl_d3_rev										sw_pad_ctl_d3_cls			
W																
Reset	0	0	0	0	1	0	1	0	0	0	1	1	0	0	1	0

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	sw_pad_ctl_d3_cls						sw_pad_ctl_d3_spl									
W																
Reset	1	0	0	0	1	1	0	0	1	0	1	0	0	0	1	1

Figure 4-96. Register Description sw_pad_ctl_d3_rev_d3_cls_d3_spl

Absolute: 0x43FA_C174 Access: User Read/Write

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R			sw_pad_ctl_read										sw_pad_ctl_vsync3			
W																
Reset	0	0	0	0	1	0	1	0	0	0	1	1	0	1	1	0

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	sw_pad_ctl_vsync3						sw_pad_ctl_contrast									
W																
Reset	1	0	0	0	1	1	0	0	1	0	1	0	0	0	1	1

Figure 4-97. Register Description sw_pad_ctl_read_vsync3_contrast

Absolute: 0x43FA_C178 Access: User Read/Write

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R			sw_pad_ctl_ser_rs										sw_pad_ctl_par_rs			
W																
Reset	0	0	0	0	1	0	1	0	0	0	1	1	0	0	1	0

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	sw_pad_ctl_par_rs						sw_pad_ctl_write									
W																
Reset	1	0	0	0	1	1	0	0	1	0	1	0	0	0	1	1

Figure 4-98. Register Description sw_pad_ctl_ser_rs_par_rs_write

Absolute: 0x43FA_C17C Access: User Read/Write

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R			sw_pad_ctl_sd_d_clk										sw_pad_ctl_lcs0			
W																
Reset	0	0	0	0	1	0	1	0	0	0	1	1	0	0	1	0

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	sw_pad_ctl_lcs0						sw_pad_ctl_lcs1									
W																
Reset	1	0	0	0	1	1	0	0	1	0	1	0	0	0	1	1

Figure 4-99. Register Description sw_pad_ctl_sd_d_clk_lcs0_lcs1

Absolute: 0x43FA_C180 Access: User Read/Write

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R			sw_pad_ctl_drdy0										sw_pad_ctl_sd_d_i			
W																
Reset	0	0	0	0	1	0	1	0	0	0	1	1	0	0	1	0

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	sw_pad_ctl_sd_d_i						sw_pad_ctl_sd_d_io									
W																
Reset	1	0	0	0	1	1	0	0	1	0	1	0	0	0	1	1

Figure 4-100. Register Description sw_pad_ctl_drdy0_sd_d_i_sd_d_io

Absolute: 0x43FA_C184 Access: User Read/Write

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R			sw_pad_ctl_vsync0										sw_pad_ctl_hsync			
W																
Reset	0	0	0	1	1	0	1	0	0	0	1	1	0	0	1	0

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	sw_pad_ctl_hsync						sw_pad_ctl_fpshift									
W																
Reset	1	0	0	0	1	1	0	0	1	0	1	0	0	0	1	1

Figure 4-101. Register Description sw_pad_ctl_vsync0_hsync_fpshift

Absolute: 0x43FA_C188 Access: User Read/Write

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R			sw_pad_ctl_ld15										sw_pad_ctl_ld16			
W																
Reset	0	0	0	1	1	0	1	0	0	0	1	1	0	1	1	0

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	sw_pad_ctl_ld16						sw_pad_ctl_ld17									
W																
Reset	1	0	0	0	1	1	0	1	1	0	1	0	0	0	1	1

Figure 4-102. Register Description sw_pad_ctl_ld15_ld16_ld17

Absolute: 0x43FA_C18C Access: User Read/Write

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R			sw_pad_ctl_ld12										sw_pad_ctl_ld13			
W																
Reset	0	0	0	1	1	0	1	0	0	0	1	1	0	1	1	0

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	sw_pad_ctl_ld13						sw_pad_ctl_ld14									
W																
Reset	1	0	0	0	1	1	0	1	1	0	1	0	0	0	1	1

Figure 4-103. Register Description sw_pad_ctl_ld12_ld13_ld14

Absolute: 0x43FA_C190 Access: User Read/Write

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R			sw_pad_ctl_ld9										sw_pad_ctl_ld10			
W																
Reset	0	0	0	1	1	0	1	0	0	0	1	1	0	1	1	0

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	sw_pad_ctl_ld10						sw_pad_ctl_ld11									
W																
Reset	1	0	0	0	1	1	0	1	1	0	1	0	0	0	1	1

Figure 4-104. Register Description sw_pad_ctl_ld9_ld10_ld11

Absolute: 0x43FA_C194 Access: User Read/Write

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R			sw_pad_ctl_ld6										sw_pad_ctl_ld7			
W																
Reset	0	0	0	1	1	0	1	0	0	0	1	1	0	1	1	0

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	sw_pad_ctl_ld7						sw_pad_ctl_ld8									
W																
Reset	1	0	0	0	1	1	0	1	1	0	1	0	0	0	1	1

Figure 4-105. Register Description sw_pad_ctl_ld6_ld7_ld8

Absolute: 0x43FA_C198 Access: User Read/Write

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R			sw_pad_ctl_ld3										sw_pad_ctl_ld4			
W																
Reset	0	0	0	1	1	0	1	0	0	0	1	1	0	1	1	0

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	sw_pad_ctl_ld4						sw_pad_ctl_ld5									
W																
Reset	1	0	0	0	1	1	0	1	1	0	1	0	0	0	1	1

Figure 4-106. Register Description sw_pad_ctl_ld3_ld4_ld5

Absolute: 0x43FA_C19C Access: User Read/Write

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R			sw_pad_ctl_ld0										sw_pad_ctl_ld1			
W																
Reset	0	0	0	1	1	0	1	0	0	0	1	1	0	1	1	0

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	sw_pad_ctl_ld1						sw_pad_ctl_ld2									
W																
Reset	1	0	0	0	1	1	0	1	1	0	1	0	0	0	1	1

Figure 4-107. Register Description sw_pad_ctl_ld0_ld1_ld2

Absolute: 0x43FA_C1A0 Access: User Read/Write

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R			sw_pad_ctl_usbh2_nxt										sw_pad_ctl_usbh2_data0			
W																
Reset	0	0	0	1	1	0	1	0	0	0	0	0	0	1	1	0

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	sw_pad_ctl_usbh2_data0						sw_pad_ctl_usbh2_data1									
W																
Reset	1	0	0	0	0	0	0	1	1	0	1	0	0	0	0	0

Figure 4-108. Register Description sw_pad_ctl_usbh2_nxt_usbh2_data0_usbh2_data1

Absolute: 0x43FA_C1A4 Access: User Read/Write

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R			sw_pad_ctl_usbh2_clk										sw_pad_ctl_usbh2_dir			
W																
Reset	0	0	0	1	1	0	1	1	0	0	0	0	0	1	1	0

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	sw_pad_ctl_usbh2_dir						sw_pad_ctl_usbh2_stp									
W																
Reset	1	0	0	0	0	0	0	1	1	0	1	0	0	0	0	0

Figure 4-109. Register Description sw_pad_ctl_usbh2_clk_usbh2_dir_usbh2_stp

Absolute: 0x43FA_C1A8 Access: User Read/Write

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R			sw_pad_ctl_usbotg_data5										sw_pad_ctl_usbotg_data6			
W																
Reset	0	0	0	1	1	0	1	0	0	0	0	0	0	1	1	0

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	sw_pad_ctl_usbotg_data6						sw_pad_ctl_usbotg_data7									
W																
Reset	1	0	0	0	0	0	0	1	1	0	1	0	0	0	0	0

Figure 4-110. Register Description sw_pad_ctl_usbotg_data5_usbotg_data6_usbotg_data7

Absolute: 0x43FA_C1AC Access: User Read/Write

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R			sw_pad_ctl_usbotg_data2										sw_pad_ctl_usbotg_data3			
W																
Reset	0	0	0	1	1	0	1	0	0	0	0	0	0	1	1	0

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	sw_pad_ctl_usbotg_data3						sw_pad_ctl_usbotg_data4									
W																
Reset	1	0	0	0	0	0	0	1	1	0	1	0	0	0	0	0

Figure 4-111. Register Description sw_pad_ctl_usbotg_data2_usbotg_data3_usbotg_data4

Absolute: 0x43FA_C1B0 Access: User Read/Write

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R			sw_pad_ctl_usbotg_nxt										sw_pad_ctl_usbotg_data0			
W																
Reset	0	0	0	1	1	0	1	0	0	0	0	0	0	1	1	0

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	sw_pad_ctl_usbotg_data0						sw_pad_ctl_usbotg_data1									
W																
Reset	1	0	0	0	0	0	0	1	1	0	1	0	0	0	0	0

Figure 4-112. Register Description sw_pad_ctl_usbotg_nxt_usbotg_data0_usbotg_data1

Absolute: 0x43FA_C1B4 Access: User Read/Write

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R			sw_pad_ctl_usbotg_clk										sw_pad_ctl_usbotg_dir			
W																
Reset	0	0	0	1	1	0	1	1	0	0	0	0	0	1	1	0

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	sw_pad_ctl_usbotg_dir						sw_pad_ctl_usbotg_stp									
W																
Reset	1	0	0	0	0	0	0	1	1	0	1	0	0	0	0	0

Figure 4-113. Register Description sw_pad_ctl_usbotg_clk_usbotg_dir_usbotg_stp

Absolute: 0x43FA_C1B8 Access: User Read/Write

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R			sw_pad_ctl_usb_pwr										sw_pad_ctl_usb_oc			
W																
Reset	0	0	0	1	1	0	1	0	0	0	0	0	0	1	1	0

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	sw_pad_ctl_usb_oc						sw_pad_ctl_usb_byp									
W																
Reset	1	0	0	0	0	0	0	1	1	0	1	0	0	0	0	0

Figure 4-114. Register Description sw_pad_ctl_usb_pwr_usb_oc_usb_byp

Absolute: 0x43FA_C1BC Access: User Read/Write

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R			sw_pad_ctl_trstb										sw_pad_ctl_de_b			
W																
Reset	0	0	0	1	1	0	1	0	0	0	0	0	0	1	1	0

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	sw_pad_ctl_de_b						sw_pad_ctl_sjc_mod									
W																
Reset	1	0	0	0	0	0	0	1	1	0	1	0	0	0	0	0

Figure 4-115. Register Description sw_pad_ctl_trstb_de_b_sjc_mod

Absolute: 0x43FA_C1C0 Access: User Read/Write

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R			sw_pad_ctl_tms										sw_pad_ctl_tdi			
W																
Reset	0	0	0	1	1	0	1	1	0	0	0	0	0	1	1	0

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	sw_pad_ctl_tdi						sw_pad_ctl_tdo									
W																
Reset	1	1	0	0	0	0	0	0	1	0	1	0	0	0	1	1

Figure 4-116. Register Description sw_pad_ctl_tms_tdi_tdo

Absolute: 0x43FA_C1C4 Access: User Read/Write

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R			sw_pad_ctl_key_col7										sw_pad_ctl_rtck			
W																
Reset	0	0	0	1	1	0	1	0	0	0	0	0	0	0	1	0

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	sw_pad_ctl_rtck						sw_pad_ctl_tck									
W																
Reset	0	0	0	0	1	1	0	1	1	0	0	1	0	0	0	0

Figure 4-117. Register Description sw_pad_ctl_key_col7_rtck_tck

Absolute: 0x43FA_C1C8 Access: User Read/Write

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R			sw_pad_ctl_key_col4										sw_pad_ctl_key_col5			
W																
Reset	0	0	0	1	1	0	1	0	0	0	0	0	0	1	1	0

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	sw_pad_ctl_key_col5						sw_pad_ctl_key_col6									
W																
Reset	1	0	0	0	0	0	0	1	1	0	1	0	0	0	0	0

Figure 4-118. Register Description sw_pad_ctl_key_col4_key_col5_key_col6

Absolute: 0x43FA_C1CC Access: User Read/Write

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R			sw_pad_ctl_key_col1										sw_pad_ctl_key_col2			
W																
Reset	0	0	0	1	1	0	1	0	0	0	0	0	0	1	1	0

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	sw_pad_ctl_key_col2						sw_pad_ctl_key_col3									
W																
Reset	1	0	0	0	0	0	0	1	1	0	1	0	0	0	0	0

Figure 4-119. Register Description sw_pad_ctl_key_col1_key_col2_key_col3

Absolute: 0x43FA_C1D0 Access: User Read/Write

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R			sw_pad_ctl_key_row6										sw_pad_ctl_key_row7			
W																
Reset	0	0	0	1	1	0	1	0	0	0	0	0	0	1	1	0

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	sw_pad_ctl_key_row7						sw_pad_ctl_key_col0									
W																
Reset	1	0	0	0	0	0	0	1	1	0	1	0	0	0	0	0

Figure 4-120. Register Description sw_pad_ctl_key_row6_key_row7_key_col0

Absolute: 0x43FA_C1D4 Access: User Read/Write

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R			sw_pad_ctl_key_row3										sw_pad_ctl_key_row4			
W																
Reset	0	0	0	1	1	0	1	0	0	0	0	0	0	1	1	0

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	sw_pad_ctl_key_row4						sw_pad_ctl_key_row5									
W																
Reset	1	0	0	0	0	0	0	1	1	0	1	0	0	0	0	0

Figure 4-121. Register Description sw_pad_ctl_key_row3_key_row4_key_row5

Absolute: 0x43FA_C1D8 Access: User Read/Write

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R			sw_pad_ctl_key_row0										sw_pad_ctl_key_row1			
W																
Reset	0	0	0	1	1	0	1	0	0	0	0	0	0	1	1	0

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	sw_pad_ctl_key_row1						sw_pad_ctl_key_row2									
W																
Reset	1	0	0	0	0	0	0	1	1	0	1	0	0	0	0	0

Figure 4-122. Register Description sw_pad_ctl_key_row0_key_row1_key_row2

Absolute: 0x43FA_C1DC Access: User Read/Write

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R			sw_pad_ctl_rts2										sw_pad_ctl_cts2			
W																
Reset	0	0	0	1	1	0	1	0	0	0	0	0	0	1	1	0

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	sw_pad_ctl_cts2						sw_pad_ctl_batt_line									
W																
Reset	1	0	0	0	0	0	1	1	1	0	1	0	1	0	0	0

Figure 4-123. Register Description sw_pad_ctl_rts2_cts2_batt_line

Absolute: 0x43FA_C1E0 Access: User Read/Write

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R			sw_pad_ctl_dtr_dce2										sw_pad_ctl_rxd2			
W																
Reset	0	0	0	1	1	0	1	0	0	0	0	0	0	1	1	0

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	sw_pad_ctl_rxd2						sw_pad_ctl_txd2									
W																
Reset	1	0	0	0	0	0	0	1	1	0	1	0	0	0	0	0

Figure 4-124. Register Description sw_pad_ctl_dtr_dce2_rxd2_txd2

Absolute: 0x43FA_C1E4 Access: User Read/Write

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R			sw_pad_ctl_dsr_dte1										sw_pad_ctl_ri_dte1			
W																
Reset	0	0	0	1	1	0	1	0	0	0	0	0	0	1	1	0

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	sw_pad_ctl_ri_dte1						sw_pad_ctl_dcd_dte1									
W																
Reset	1	1	0	0	0	0	0	1	1	0	1	0	0	0	0	0

Figure 4-125. Register Description sw_pad_ctl_dsr_dte1_ri_dte1_dcd_dte1

Absolute: 0x43FA_C1E8 Access: User Read/Write

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R			sw_pad_ctl_ri_dce1										sw_pad_ctl_dcd_dce1			
W																
Reset	0	0	0	1	1	0	1	0	0	0	0	0	0	1	1	0

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	sw_pad_ctl_dcd_dce1						sw_pad_ctl_dtr_dte1									
W																
Reset	1	0	0	0	0	0	0	1	1	0	1	1	0	0	0	0

Figure 4-126. Register Description sw_pad_ctl_ri_dce1_dcd_dce1_dtr_dte1

Absolute: 0x43FA_C1EC Access: User Read/Write

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R			sw_pad_ctl_cts1										sw_pad_ctl_dtr_dce1			
W																
Reset	0	0	0	1	1	0	1	0	0	0	0	0	0	1	1	0

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	sw_pad_ctl_dtr_dce1						sw_pad_ctl_dsr_dce1									
W																
Reset	1	0	0	0	0	0	0	1	1	0	1	0	0	0	0	0

Figure 4-127. Register Description sw_pad_ctl_cts1_dtr_dce1_dsr_dce1

Absolute: 0x43FA_C1F0 Access: User Read/Write

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R			sw_pad_ctl_rxd1										sw_pad_ctl_txd1			
W																
Reset	0	0	0	1	1	0	1	0	0	0	0	0	0	1	1	0

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	sw_pad_ctl_txd1						sw_pad_ctl_rts1									
W																
Reset	1	0	0	0	0	0	0	1	1	0	1	0	0	0	0	0

Figure 4-128. Register Description sw_pad_ctl_rxd1_txd1_rts1

Absolute: 0x43FA_C1F4 Access: User Read/Write

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R			sw_pad_ctl_cspi2_ss2										sw_pad_ctl_cspi2_sclk			
W																
Reset	0	0	0	1	1	0	1	1	0	0	0	0	0	1	1	0

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	sw_pad_ctl_cspi2_sclk						sw_pad_ctl_cspi2_spi_rdy									
W																
Reset	1	1	0	0	0	0	0	1	1	0	1	0	0	0	0	0

Figure 4-129. Register Description sw_pad_ctl_cspi2_ss2_cspi2_sclk_cspi2_spi_rdy

Absolute: 0x43FA_C1F8 Access: User Read/Write

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R			sw_pad_ctl_cspi2_miso										sw_pad_ctl_cspi2_ss0			
W																
Reset	0	0	0	1	1	0	1	1	0	0	0	0	0	1	1	0

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	sw_pad_ctl_cspi2_ss0						sw_pad_ctl_cspi2_ss1									
W																
Reset	1	0	0	0	0	0	0	1	1	0	1	0	0	0	0	0

Figure 4-130. Register Description sw_pad_ctl_cspi2_miso_cspi2_ss0_cspi2_ss1

Absolute: 0x43FA_C1FC Access: User Read/Write

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R			sw_pad_ctl_cspi1_sclk										sw_pad_ctl_cspi1_spi_rdy			
W																
Reset	0	0	0	1	1	0	1	1	0	0	0	0	0	1	1	0

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	sw_pad_ctl_cspi1_spi_rdy						sw_pad_ctl_cspi2_mosi									
W																
Reset	1	0	0	0	0	0	0	1	1	0	1	1	0	0	0	0

Figure 4-131. Register Description sw_pad_ctl_cspi1_sclk_cspi1_spi_rdy_cspi2_mosi

Absolute: 0x43FA_C200 Access: User Read/Write

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R			sw_pad_ctl_cspi1_ss0										sw_pad_ctl_cspi1_ss1			
W																
Reset	0	0	0	1	1	0	1	0	0	0	0	0	0	1	1	0

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	sw_pad_ctl_cspi1_ss1						sw_pad_ctl_cspi1_ss2									
W																
Reset	1	0	0	0	0	0	0	1	1	0	1	0	0	0	0	0

Figure 4-132. Register Description sw_pad_ctl_cspi1_ss0_cspi1_ss1_cspi1_ss2

Absolute: 0x43FA_C204 Access: User Read/Write

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R			sw_pad_ctl_sfs6										sw_pad_ctl_cspi1_mosi			
W																
Reset	0	0	0	1	1	0	1	0	0	0	0	0	0	1	1	0

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	sw_pad_ctl_cspi1_mosi						sw_pad_ctl_cspi1_miso									
W																
Reset	1	0	0	0	0	0	0	1	1	0	1	0	0	0	0	0

Figure 4-133. Register Description sw_pad_ctl_sfs6_cspi1_mosi_cspi1_miso

Absolute: 0x43FA_C208 Access: User Read/Write

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R			sw_pad_ctl_stxd6										sw_pad_ctl_srxd6			
W																
Reset	0	0	0	1	1	0	1	0	0	0	0	0	0	1	1	0

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	sw_pad_ctl_srxd6						sw_pad_ctl_sck6									
W																
Reset	1	0	0	0	0	0	0	1	1	0	1	1	0	0	0	0

Figure 4-134. Register Description sw_pad_ctl_stxd6_srxd6_sck6

Absolute: 0x43FA_C20C Access: User Read/Write

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R			sw_pad_ctl_srxd5										sw_pad_ctl_sck5			
W																
Reset	0	0	0	1	1	0	1	0	0	0	0	0	0	1	1	0

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	sw_pad_ctl_sck5						sw_pad_ctl_sfs5									
W																
Reset	1	1	0	0	0	0	0	1	1	0	1	0	0	0	0	0

Figure 4-135. Register Description sw_pad_ctl_srxd5_sck5_sfs5

Absolute: 0x43FA_C210 Access: User Read/Write

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R			sw_pad_ctl_sck4										sw_pad_ctl_sfs4			
W																
Reset	0	0	0	1	1	0	1	1	0	0	0	0	0	1	1	0

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	sw_pad_ctl_sfs4						sw_pad_ctl_stxd5									
W																
Reset	1	0	0	0	0	0	0	1	1	0	1	0	0	0	0	0

Figure 4-136. Register Description sw_pad_ctl_sck4_sfs4_stxd5

Absolute: 0x43FA_C214 Access: User Read/Write

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R			sw_pad_ctl_sfs3										sw_pad_ctl_stxd4			
W																
Reset	0	0	0	1	1	0	1	0	0	0	0	0	0	1	1	0

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	sw_pad_ctl_stxd4						sw_pad_ctl_srxd4									
W																
Reset	1	0	0	0	0	0	0	1	1	0	1	0	0	0	0	0

Figure 4-137. Register Description sw_pad_ctl_sfs3_stxd4_srxd4

Absolute: 0x43FA_C218 Access: User Read/Write

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R			sw_pad_ctl_stxd3										sw_pad_ctl_srxd3			
W																
Reset	0	0	0	1	1	0	1	0	0	0	0	0	0	1	1	0

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	sw_pad_ctl_srxd3						sw_pad_ctl_sck3									
W																
Reset	1	0	0	0	0	0	0	1	1	0	1	1	0	0	0	0

Figure 4-138. Register Description sw_pad_ctl_stxd3_srxd3_sck3

Absolute: 0x43FA_C21C Access: User Read/Write

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R			sw_pad_ctl_csi_pixclk										sw_pad_ctl_i2c_clk			
W																
Reset	0	0	0	1	0	0	1	1	0	0	1	1	0	1	1	0

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	sw_pad_ctl_i2c_clk						sw_pad_ctl_i2c_dat									
W																
Reset	1	1	0	0	0	0	0	1	1	0	1	1	0	0	0	0

Figure 4-139. Register Description sw_pad_ctl_csi_pixclk_i2c_clk_i2c_dat

Absolute: 0x43FA_C220 Access: User Read/Write

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R			sw_pad_ctl_csi_mclk										sw_pad_ctl_csi_vsync			
W																
Reset	0	0	0	1	0	0	1	0	0	0	1	1	0	1	0	0

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	sw_pad_ctl_csi_vsync						sw_pad_ctl_csi_hsync									
W																
Reset	1	0	0	0	1	1	0	1	0	0	1	0	0	0	1	1

Figure 4-140. Register Description sw_pad_ctl_csi_mclk_csi_vsync_csi_hsync

Absolute: 0x43FA_C224 Access: User Read/Write

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R			sw_pad_ctl_csi_d13										sw_pad_ctl_csi_d14			
W																
Reset	0	0	0	1	0	0	1	0	0	0	1	1	0	1	0	0

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	sw_pad_ctl_csi_d14						sw_pad_ctl_csi_d15									
W																
Reset	1	0	0	0	1	1	0	1	0	0	1	0	0	0	1	1

Figure 4-141. Register Description sw_pad_ctl_csi_d13_csi_d14_csi_d15

Absolute: 0x43FA_C228 Access: User Read/Write

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R			sw_pad_ctl_csi_d10										sw_pad_ctl_csi_d11			
W																
Reset	0	0	0	1	0	0	1	0	0	0	1	1	0	1	0	0

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	sw_pad_ctl_csi_d11						sw_pad_ctl_csi_d12									
W																
Reset	1	0	0	0	1	1	0	1	0	0	1	0	0	0	1	1

Figure 4-142. Register Description sw_pad_ctl_csi_d10_csi_d11_csi_d12

Absolute: 0x43FA_C22C Access: User Read/Write

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R			sw_pad_ctl_csi_d7										sw_pad_ctl_csi_d8			
W																
Reset	0	0	0	1	0	0	1	0	0	0	1	1	0	1	0	0

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	sw_pad_ctl_csi_d8						sw_pad_ctl_csi_d9									
W																
Reset	1	0	0	0	1	1	0	1	0	0	1	0	0	0	1	1

Figure 4-143. Register Description sw_pad_ctl_csi_d7_csi_d8_csi_d9

Absolute: 0x43FA_C230 Access: User Read/Write

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R			sw_pad_ctl_csi_d4										sw_pad_ctl_csi_d5			
W																
Reset	0	0	0	1	0	0	1	0	0	0	1	1	0	1	0	0

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	sw_pad_ctl_csi_d5						sw_pad_ctl_csi_d6									
W																
Reset	1	0	0	0	1	1	0	1	0	0	1	0	0	0	1	1

Figure 4-144. Register Description sw_pad_ctl_csi_d4_csi_d5_csi_d6

Absolute: 0x43FA_C234 Access: User Read/Write

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R			sw_pad_ctl_pc_poe										sw_pad_ctl_m_request			
W																
Reset	0	0	0	0	1	0	1	0	0	0	1	0	0	0	1	0

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	sw_pad_ctl_m_request						sw_pad_ctl_m_grant									
W																
Reset	1	0	0	0	0	0	0	1	1	0	1	0	0	0	0	0

Figure 4-145. Register Description sw_pad_ctl_pc_poe_m_request_m_grant

Absolute: 0x43FA_C238 Access: User Read/Write

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R			sw_pad_ctl_pc_rst										sw_pad_ctl_iois16			
W																
Reset	0	0	0	1	1	0	1	0	0	0	1	0	0	1	1	0

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	sw_pad_ctl_iois16						sw_pad_ctl_pc_rw_b									
W																
Reset	1	0	0	0	1	0	0	1	1	0	1	0	0	0	1	0

Figure 4-146. Register Description sw_pad_ctl_pc_rst_iois16_pc_rw_b

Absolute: 0x43FA_C23C Access: User Read/Write

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R			sw_pad_ctl_pc_vs2										sw_pad_ctl_pc_bvd1			
W																
Reset	0	0	0	1	1	0	1	0	0	0	1	0	0	1	1	0

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	sw_pad_ctl_pc_bvd1						sw_pad_ctl_pc_bvd2									
W																
Reset	1	0	0	0	1	0	0	1	1	0	1	0	0	0	1	0

Figure 4-147. Register Description sw_pad_ctl_pc_vs2_pc_bvd1_pc_bvd2

Absolute: 0x43FA_C240 Access: User Read/Write

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R			sw_pad_ctl_pc_ready										sw_pad_ctl_pc_pwron			
W																
Reset	0	0	0	1	1	0	1	0	0	0	1	0	0	1	1	0

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	sw_pad_ctl_pc_pwron						sw_pad_ctl_pc_vs1									
W																
Reset	0	0	0	0	1	0	0	1	1	0	1	0	0	0	1	0

Figure 4-148. Register Description sw_pad_ctl_pc_ready_pc_pwron_pc_vs1

Absolute: 0x43FA_C244 Access: User Read/Write

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R			sw_pad_ctl_pc_cd1_b										sw_pad_ctl_pc_cd2_b			
W																
Reset	0	0	0	1	1	0	1	0	0	0	1	0	0	1	1	0

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	sw_pad_ctl_pc_cd2_b						sw_pad_ctl_pc_wait_b									
W																
Reset	1	0	0	0	1	0	0	1	1	0	1	0	0	0	1	0

Figure 4-149. Register Description sw_pad_ctl_pc_cd1_b_pc_cd2_b_pc_wait_b

Absolute: 0x43FA_C248 Access: User Read/Write

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R			sw_pad_ctl_d2										sw_pad_ctl_d1			
W																
Reset	0	0	0	1	0	0	1	0	0	1	1	1	0	1	0	0

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	sw_pad_ctl_d1						sw_pad_ctl_d0									
W																
Reset	1	0	0	1	1	1	0	1	0	0	1	0	0	1	1	1

Figure 4-150. Register Description sw_pad_ctl_d2_d1_d0

Absolute: 0x43FA_C24C Access: User Read/Write

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R			sw_pad_ctl_d5										sw_pad_ctl_d4			
W																
Reset	0	0	0	1	0	0	1	0	0	1	1	1	0	1	0	0

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	sw_pad_ctl_d4						sw_pad_ctl_d3									
W																
Reset	1	0	0	1	1	1	0	1	0	0	1	0	0	1	1	1

Figure 4-151. Register Description sw_pad_ctl_d5_d4_d3

Absolute: 0x43FA_C250 Access: User Read/Write

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R			sw_pad_ctl_d8										sw_pad_ctl_d7			
W																
Reset	0	0	0	1	0	0	1	0	0	1	1	1	0	1	0	0

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	sw_pad_ctl_d7						sw_pad_ctl_d6									
W																
Reset	1	0	0	1	1	1	0	1	0	0	1	0	0	1	1	1

Figure 4-152. Register Description sw_pad_ctl_d8_d7_d6

Absolute: 0x43FA_C254 Access: User Read/Write

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R			sw_pad_ctl_d11										sw_pad_ctl_d10			
W																
Reset	0	0	0	1	0	0	1	0	0	1	1	1	0	1	0	0

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	sw_pad_ctl_d10						sw_pad_ctl_d9									
W																
Reset	1	0	0	1	1	1	0	1	0	0	1	0	0	1	1	1

Figure 4-153. Register Description sw_pad_ctl_d11_d10_d9

Absolute: 0x43FA_C258 Access: User Read/Write

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R			sw_pad_ctl_d14										sw_pad_ctl_d13			
W																
Reset	0	0	0	1	0	0	1	0	0	1	1	1	0	1	0	0

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	sw_pad_ctl_d13						sw_pad_ctl_d12									
W																
Reset	1	0	0	1	1	1	0	1	0	0	1	0	0	1	1	1

Figure 4-154. Register Description sw_pad_ctl_d14_d13_d12

Absolute: 0x43FA_C25C Access: User Read/Write

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R			sw_pad_ctl_nfce_b										sw_pad_ctl_nfrb			
W																
Reset	0	0	0	1	1	0	1	0	0	0	1	1	0	1	1	0

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	sw_pad_ctl_nfrb						sw_pad_ctl_d15									
W																
Reset	1	0	0	0	1	1	0	1	0	0	1	0	0	1	1	1

Figure 4-155. Register Description sw_pad_ctl_nfce_b_nfrb_d15

Absolute: 0x43FA_C260 Access: User Read/Write

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R			sw_pad_ctl_nfale										sw_pad_ctl_nfcle			
W																
Reset	0	0	0	1	1	0	1	0	0	0	1	1	0	1	1	0

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	sw_pad_ctl_nfcle						sw_pad_ctl_nfwp_b									
W																
Reset	1	0	0	0	1	1	0	1	1	0	1	0	0	0	1	1

Figure 4-156. Register Description sw_pad_ctl_nfale_nfcle_nfwp_b

Absolute: 0x43FA_C264 Access: User Read/Write

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R			sw_pad_ctl_sdqs3										sw_pad_ctl_nfwe_b			
W																
Reset	0	0	0	1	1	0	0	0	0	0	0	1	0	1	1	0

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	sw_pad_ctl_nfwe_b						sw_pad_ctl_nfre_b									
W																
Reset	0	0	0	0	1	1	0	1	1	0	1	0	0	0	1	1

Figure 4-157. Register Description sw_pad_ctl_sdqs3_nfwe_b_nfre_b

Absolute: 0x43FA_C268 Access: User Read/Write

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R			sw_pad_ctl_sdqs0										sw_pad_ctl_sdqs1			
W																
Reset	0	0	0	1	1	0	0	0	0	0	0	1	0	1	1	0

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	sw_pad_ctl_sdqs1						sw_pad_ctl_sdqs2									
W																
Reset	0	0	0	0	0	1	0	1	1	0	0	0	0	0	0	1

Figure 4-158. Register Description sw_pad_ctl_sdqs0_sdqs1_sdqs2

Absolute: 0x43FA_C26C Access: User Read/Write

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R			sw_pad_ctl_sdcke1										sw_pad_ctl_sdclk*			
W																
Reset	0	0	0	1	0	0	1	0	0	0	0	1	1	0	1	0

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	sw_pad_ctl_sdclk*						Reserved									
W																
Reset	1	0	0	1	1	1	0	1	1	0	1	0	0	0	0	0

*Bits 10–19 control the differential output pair SDCLK and $\overline{\text{SDCLK}}$.

Figure 4-159. Register Description sw_pad_ctl_sdcke1_sdclk_sdclk_b

Absolute: 0x43FA_C270 Access: User Read/Write

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R			sw_pad_ctl_cas										sw_pad_ctl_sdwe			
W																
Reset	0	0	0	1	0	0	1	0	0	1	1	1	0	1	0	0

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	sw_pad_ctl_sdwe						sw_pad_ctl_sdcke0									
W																
Reset	1	0	0	0	0	1	0	1	0	0	1	0	0	0	0	1

Figure 4-160. Register Description sw_pad_ctl_cas_sdwe_sdcke0

Absolute: 0x43FA_C274 Access: User Read/Write

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R			sw_pad_ctl_bclk										sw_pad_ctl_rw			
W																
Reset	0	0	1	0	1	0	1	0	0	0	1	1	0	0	1	0

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	sw_pad_ctl_rw						sw_pad_ctl_ras									
W																
Reset	1	0	0	0	1	1	0	1	0	0	1	0	0	1	1	1

Figure 4-161. Register Description sw_pad_ctl_bclk_rw_ras

Absolute: 0x43FA_C278 Access: User Read/Write

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R			sw_pad_ctl_cs5										sw_pad_ctl_ecb			
W																
Reset	0	0	0	0	1	0	1	0	0	0	1	1	0	1	1	0

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	sw_pad_ctl_ecb						sw_pad_ctl_lba									
W																
Reset	1	0	0	0	1	1	0	0	1	0	1	0	0	0	1	1

Figure 4-162. Register Description sw_pad_ctl_cs5_ecb_lba

Absolute: 0x43FA_C27C Access: User Read/Write

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R			sw_pad_ctl_cs2										sw_pad_ctl_cs3			
W																
Reset	0	0	0	1	0	0	1	0	0	1	1	1	0	1	0	0

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	sw_pad_ctl_cs3						sw_pad_ctl_cs4									
W																
Reset	1	0	0	1	1	1	0	0	1	0	1	0	0	0	1	1

Figure 4-163. Register Description sw_pad_ctl_cs2_cs3_cs4

Absolute: 0x43FA_C280 Access: User Read/Write

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R			sw_pad_ctl_oe										sw_pad_ctl_cs0			
W																
Reset	0	0	0	0	1	0	1	0	0	0	1	1	0	0	1	0

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	sw_pad_ctl_cs0						sw_pad_ctl_cs1									
W																
Reset	1	0	0	0	1	1	0	0	1	0	1	0	0	0	1	1

Figure 4-164. Register Description sw_pad_ctl_oe_cs0_cs1

Absolute: 0x43FA_C284 Access: User Read/Write

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R			sw_pad_ctl_dqm3										sw_pad_ctl_eb0			
W																
Reset	0	0	0	1	0	0	1	0	0	1	1	1	0	0	1	0

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	sw_pad_ctl_eb0						sw_pad_ctl_eb1									
W																
Reset	1	0	0	0	1	1	0	0	1	0	1	0	0	0	1	1

Figure 4-165. Register Description sw_pad_ctl_dqm3_eb0_eb1

Absolute: 0x43FA_C288 Access: User Read/Write

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R			sw_pad_ctl_dqm0										sw_pad_ctl_dqm1			
W																
Reset	0	0	0	1	0	0	1	0	0	1	1	1	0	1	0	0

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	sw_pad_ctl_dqm1						sw_pad_ctl_dqm2									
W																
Reset	1	0	0	1	1	1	0	1	0	0	1	0	0	1	1	1

Figure 4-166. Register description sw_pad_ctl_dqm0_dqm1_dqm2

Absolute: 0x43FA_C28C Access: User Read/Write

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R			sw_pad_ctl_sd29										sw_pad_ctl_sd30			
W																
Reset	0	0	0	1	0	0	1	0	0	1	1	1	0	1	0	0

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	sw_pad_ctl_sd30						sw_pad_ctl_sd31									
W																
Reset	1	0	0	1	1	1	0	1	0	0	1	0	0	1	1	1

Figure 4-167. Register Description sw_pad_ctl_sd29_sd30_sd31

Absolute: 0x43FA_C290 Access: User Read/Write

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R			sw_pad_ctl_sd26										sw_pad_ctl_sd27			
W																
Reset	0	0	0	1	0	0	1	0	0	1	1	1	0	1	0	0

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	sw_pad_ctl_sd27						sw_pad_ctl_sd28									
W																
Reset	1	0	0	1	1	1	0	1	0	0	1	0	0	1	1	1

Figure 4-168. Register Description sw_pad_ctl_sd26_sd27_sd28

Absolute: 0x43FA_C294 Access: User Read/Write

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R			sw_pad_ctl_sd23										sw_pad_ctl_sd24			
W																
Reset	0	0	0	1	0	0	1	0	0	1	1	1	0	1	0	0

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	sw_pad_ctl_sd24						sw_pad_ctl_sd25									
W																
Reset	1	0	0	1	1	1	0	1	0	0	1	0	0	1	1	1

Figure 4-169. Register Description sw_pad_ctl_sd23_sd24_sd25

Absolute: 0x43FA_C298 Access: User Read/Write

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R			sw_pad_ctl_sd20										sw_pad_ctl_sd21			
W																
Reset	0	0	0	1	0	0	1	0	0	1	1	1	0	1	0	0

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	sw_pad_ctl_sd21						sw_pad_ctl_sd22									
W																
Reset	1	0	0	1	1	1	0	1	0	0	1	0	0	1	1	1

Figure 4-170. Register Description sw_pad_ctl_sd20_sd21_sd22

Absolute: 0x43FA_C29C Access: User Read/Write

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R			sw_pad_ctl_sd17										sw_pad_ctl_sd18			
W																
Reset	0	0	0	1	0	0	1	0	0	1	1	1	0	1	0	0

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	sw_pad_ctl_sd18						sw_pad_ctl_sd19									
W																
Reset	1	0	0	1	1	1	0	1	0	0	1	0	0	1	1	1

Figure 4-171. Register Description sw_pad_ctl_sd17_sd18_sd19

Absolute: 0x43FA_C2A0 Access: User Read/Write

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R			sw_pad_ctl_sd14										sw_pad_ctl_sd15			
W																
Reset	0	0	0	1	0	0	1	0	0	1	1	1	0	1	0	0

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	sw_pad_ctl_sd15						sw_pad_ctl_sd16									
W																
Reset	1	0	0	1	1	1	0	1	0	0	1	0	0	1	1	1

Figure 4-172. Register Description sw_pad_ctl_sd14_sd15_sd16

Absolute: 0x43FA_C2A4 Access: User Read/Write

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R			sw_pad_ctl_sd11										sw_pad_ctl_sd12			
W																
Reset	0	0	0	1	0	0	1	0	0	1	1	1	0	1	0	0

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	sw_pad_ctl_sd12						sw_pad_ctl_sd13									
W																
Reset	1	0	0	1	1	1	0	1	0	0	1	0	0	1	1	1

Figure 4-173. Register Description sw_pad_ctl_sd11_sd12_sd13

Absolute: 0x43FA_C2A8 Access: User Read/Write

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R			sw_pad_ctl_sd8										sw_pad_ctl_sd9			
W																
Reset	0	0	0	1	0	0	1	0	0	1	1	1	0	1	0	0

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	sw_pad_ctl_sd9						sw_pad_ctl_sd10									
W																
Reset	1	0	0	1	1	1	0	1	0	0	1	0	0	1	1	1

Figure 4-174. Register Description sw_pad_ctl_sd8_sd9_sd10

Absolute: 0x43FA_C2AC Access: User Read/Write

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R			sw_pad_ctl_sd5										sw_pad_ctl_sd6			
W																
Reset	0	0	0	1	0	0	1	0	0	1	1	1	0	1	0	0

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	sw_pad_ctl_sd6						sw_pad_ctl_sd7									
W																
Reset	1	0	0	1	1	1	0	1	0	0	1	0	0	1	1	1

Figure 4-175. Register Description sw_pad_ctl_sd5_sd6_sd7

Absolute: 0x43FA_C2B0 Access: User Read/Write

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R			sw_pad_ctl_sd2										sw_pad_ctl_sd3			
W																
Reset	0	0	0	1	0	0	1	0	0	1	1	1	0	1	0	0

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	sw_pad_ctl_sd3						sw_pad_ctl_sd4									
W																
Reset	1	0	0	1	1	1	0	1	0	0	1	0	0	1	1	1

Figure 4-176. Register Description sw_pad_ctl_sd2_sd3_sd4

Absolute: 0x43FA_C2B4 Access: User Read/Write

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R			sw_pad_ctl_sdba0										sw_pad_ctl_sd0			
W																
Reset	0	0	0	0	1	0	1	0	0	0	0	1	0	1	0	0

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	sw_pad_ctl_sd0						sw_pad_ctl_sd1									
W																
Reset	1	0	0	1	1	1	0	1	0	0	1	0	0	1	1	1

Figure 4-177. Register Description sw_pad_ctl_sdba0_sd0_sd1

Absolute: 0x43FA_C2B8 Access: User Read/Write

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R			sw_pad_ctl_a24										sw_pad_ctl_a25			
W																
Reset	0	0	0	0	1	0	1	0	0	1	1	1	0	0	1	0

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	sw_pad_ctl_a25						sw_pad_ctl_sdba1									
W																
Reset	1	0	0	1	1	1	0	0	1	0	1	0	0	0	0	1

Figure 4-178. Register Description sw_pad_ctl_a24_a25_sdba1

Absolute: 0x43FA_C2BC Access: User Read/Write

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R			sw_pad_ctl_a21										sw_pad_ctl_a22			
W																
Reset	0	0	0	0	1	0	1	0	0	1	1	1	0	0	1	0

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	sw_pad_ctl_a22						sw_pad_ctl_a23									
W																
Reset	1	0	0	1	1	1	0	0	1	0	1	0	0	1	1	1

Figure 4-179. Register Description sw_pad_ctl_a21_a22_a23

Absolute: 0x43FA_C2C0 Access: User Read/Write

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R			sw_pad_ctl_a18										sw_pad_ctl_a19			
W																
Reset	0	0	0	0	1	0	1	0	0	1	1	1	0	0	1	0

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	sw_pad_ctl_a19						sw_pad_ctl_a20									
W																
Reset	1	0	0	1	1	1	0	0	1	0	1	0	0	1	1	1

Figure 4-180. Register Description sw_pad_ctl_a18_a19_a20

Absolute: 0x43FA_C2C4 Access: User Read/Write

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R			sw_pad_ctl_a15										sw_pad_ctl_a16			
W																
Reset	0	0	0	0	1	0	1	0	0	1	1	1	0	0	1	0

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	sw_pad_ctl_a16						sw_pad_ctl_a17									
W																
Reset	1	0	0	1	1	1	0	0	1	0	1	0	0	1	1	1

Figure 4-181. Register Description sw_pad_ctl_a15_a16_a17

Absolute: 0x43FA_C2C8 Access: User Read/Write

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R			sw_pad_ctl_a12										sw_pad_ctl_a13			
W																
Reset	0	0	0	0	1	0	1	0	0	1	1	1	0	0	1	0

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	sw_pad_ctl_a13						sw_pad_ctl_a14									
W																
Reset	1	0	0	1	1	1	0	0	1	0	1	0	0	1	1	1

Figure 4-182. Register Description sw_pad_ctl_a12_a13_a14

Absolute: 0x43FA_C2CC Access: User Read/Write

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R			sw_pad_ctl_a10										sw_pad_ctl_ma10			
W																
Reset	0	0	0	0	1	0	1	0	0	1	1	1	0	0	1	0

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	sw_pad_ctl_ma10						sw_pad_ctl_a11									
W																
Reset	1	0	0	1	1	1	0	0	1	0	1	0	0	1	1	1

Figure 4-183. Register Description sw_pad_ctl_a10_ma10_a11

Absolute: 0x43FA_C2D0 Access: User Read/Write

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R			sw_pad_ctl_a7										sw_pad_ctl_a8			
W																
Reset	0	0	0	0	1	0	1	0	0	1	1	1	0	0	1	0

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	sw_pad_ctl_a8						sw_pad_ctl_a9									
W																
Reset	1	0	0	1	1	1	0	0	1	0	1	0	0	1	1	1

Figure 4-184. Register Description sw_pad_ctl_a7_a8_a9

Absolute: 0x43FA_C2D4 Access: User Read/Write

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R			sw_pad_ctl_a4										sw_pad_ctl_a5			
W																
Reset	0	0	0	0	1	0	1	0	0	1	1	1	0	0	1	0

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	sw_pad_ctl_a5						sw_pad_ctl_a6									
W																
Reset	1	0	0	1	1	1	0	0	1	0	1	0	0	1	1	1

Figure 4-185. Register Description sw_pad_ctl_a4_a5_a6

Absolute: 0x43FA_C2D8 Access: User Read/Write

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R			sw_pad_ctl_a1										sw_pad_ctl_a2			
W																
Reset	0	0	0	0	1	0	1	0	0	1	1	1	0	0	1	0

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	sw_pad_ctl_a2						sw_pad_ctl_a3									
W																
Reset	1	0	0	1	1	1	0	0	1	0	1	0	0	1	1	1

Figure 4-186. Register Description sw_pad_ctl_a1_a2_a3

Absolute: 0x43FA_C2DC Access: User Read/Write

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R			sw_pad_ctl_vpg0										sw_pad_ctl_vpg1			
W																
Reset	0	0	0	0	1	0	1	0	0	0	0	0	0	0	1	0

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	sw_pad_ctl_vpg1						sw_pad_ctl_a0									
W																
Reset	1	0	0	0	0	0	0	0	1	0	1	0	0	1	1	1

Figure 4-187. Register Description sw_pad_ctl_vpg0_vpg1_a0

Absolute: 0x43FA_C2E0 Access: User Read/Write

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R			sw_pad_ctl_vstby										sw_pad_ctl_dvfs0			
W																
Reset	0	0	0	0	1	0	1	0	0	0	0	0	0	0	1	0

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	sw_pad_ctl_dvfs0						sw_pad_ctl_dvfs1									
W																
Reset	1	0	0	0	0	0	0	0	1	0	1	0	0	0	0	0

Figure 4-188. Register Description sw_pad_ctl_vstby_dvfs0_dvfs1

Absolute: 0x43FA_C2E4 Access: User Read/Write

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R			sw_pad_ctl_boot_mode4										sw_pad_ctl_ckil			
W																
Reset	0	0	0	0	1	0	1	0	0	0	0	0	0	0	1	0

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	sw_pad_ctl_ckil						sw_pad_ctl_power_fail									
W																
Reset	1	1	0	0	0	0	0	1	1	0	0	0	0	0	0	0

Figure 4-189. Register Description sw_pad_ctl_boot_mode4_ckil_power_fail

Absolute: 0x43FA_C2E8 Access: User Read/Write

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R			sw_pad_ctl_boot_mode1										sw_pad_ctl_boot_mode2			
W																
Reset	0	0	0	0	1	0	1	0	0	0	0	0	0	0	1	0

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	sw_pad_ctl_boot_mode2						sw_pad_ctl_boot_mode3									
W																
Reset	1	0	0	0	0	0	0	0	1	0	1	0	0	0	0	0

Figure 4-190. Register Description sw_pad_ctl_boot_mode1_boot_mode2_boot_mode3

Absolute: 0x43FA_C2EC Access: User Read/Write

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R			sw_pad_ctl_por_b										sw_pad_ctl_clko			
W																
Reset	0	0	0	1	1	0	1	1	0	0	0	0	0	0	1	0

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	sw_pad_ctl_clko						sw_pad_ctl_boot_mode0									
W																
Reset	1	0	0	1	1	1	0	0	1	0	1	0	0	0	0	0

Figure 4-191. Register Description sw_pad_ctl_por_b_clko_boot_mode0

Absolute: 0x43FA_C2F0 Access: User Read/Write

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R			sw_pad_ctl_simpd0										sw_pad_ctl_ckih			
W																
Reset	0	0	0	1	1	0	1	0	0	0	0	0	0	0	1	0

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	sw_pad_ctl_ckih						sw_pad_ctl_reset_in_b									
W																
Reset	1	1	0	0	0	0	0	1	1	0	1	1	0	0	0	0

Figure 4-192. Register Description sw_pad_ctl_simpd0_ckih_reset_in_b

Absolute: 0x43FA_C2F4 Access: User Read/Write

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R			sw_pad_ctl_sven0										sw_pad_ctl_stx0			
W																
Reset	0	0	0	1	1	0	1	0	0	0	0	0	1	1	1	0

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	sw_pad_ctl_stx0						sw_pad_ctl_srx0									
W																
Reset	1	0	0	0	0	0	0	1	1	0	1	0	0	0	0	0

Figure 4-193. Register Description sw_pad_ctl_sven0_stx0_srx0

Absolute: 0x43FA_C2F8 Access: User Read/Write

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R			sw_pad_ctl_gpio3_1										sw_pad_ctl_sclk0			
W																
Reset	0	0	0	1	1	0	1	0	0	0	0	0	0	1	1	0

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	sw_pad_ctl_sclk0						sw_pad_ctl_srst0									
W																
Reset	1	0	0	0	0	0	0	1	1	0	1	0	0	0	0	0

Figure 4-194. Register Description sw_pad_ctl_gpio3_1_sclk0_srst0

Absolute: 0x43FA_C2FC Access: User Read/Write

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R			sw_pad_ctl_gpio1_5										sw_pad_ctl_gpio1_6			
W																
Reset	0	0	0	1	1	0	1	0	0	0	0	0	0	1	1	0

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	sw_pad_ctl_gpio1_6						sw_pad_ctl_gpio3_0									
W																
Reset	1	0	0	0	0	0	0	1	1	0	1	0	0	0	0	0

Figure 4-195. Register Description sw_pad_ctl_gpio1_5_gpio1_6_gpio3_0

Absolute: 0x43FA_C300 Access: User Read/Write

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R			sw_pad_ctl_gpio1_2										sw_pad_ctl_gpio1_3			
W																
Reset	0	0	0	1	1	0	1	0	0	0	0	0	0	1	1	0

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	sw_pad_ctl_gpio1_3						sw_pad_ctl_gpio1_4									
W																
Reset	1	0	0	0	0	0	0	1	1	0	1	0	0	0	0	0

Figure 4-196. Register Description sw_pad_ctl_gpio1_2_gpio1_3_gpio1_4

Absolute: 0x43FA_C304 Access: User Read/Write

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R			sw_pad_ctl_pwmo										sw_pad_ctl_gpio1_0			
W																
Reset	0	0	0	0	1	0	1	1	0	0	0	0	0	1	1	0

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	sw_pad_ctl_gpio1_0						sw_pad_ctl_gpio1_1									
W																
Reset	1	0	0	0	0	0	0	1	1	0	1	0	0	0	0	0

Figure 4-197. Register Description sw_pad_ctl_pwmo_gpio1_0_gpio1_1

Absolute: 0x43FA_C308 Access: User Read/Write

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R			sw_pad_ctl_capture										sw_pad_ctl_compare			
W																
Reset	0	0	0	1	1	0	1	0	0	0	0	0	0	1	1	0

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	sw_pad_ctl_compare						sw_pad_ctl_watchdog_rst									
W																
Reset	1	0	0	0	0	0	0	1	1	0	1	0	0	0	0	0

Figure 4-198. Register Description sw_pad_ctl_capture_compare_watchdog_rst

4.4 I/O Settings

The settings for each I/O are described in Table 4-12 on page 4-119. The table includes bit descriptions for all settings and whether they are software configurable.

4.4.1 Special I/O and Exceptions for SW_PAD_CTL

Table 4-11 on page 4-116 lists the exceptions to the I/O settings shown in Table 4-12. These exception apply only to ICs that are Revision 1.2. For each of these signals, the I/O characteristics override the value shown in the corresponding SW_PAD_CTL register; thus, the SW_PAD_CTL register has no impact on these signals. In addition, the signal characteristics shown in are hardwired and are not configurable.

NOTE

Ignore the information in Table 4-11 when working with ICs with revisions previous to version 1.2.

Table 4-11. I/O Setting Exceptions and Special Pad Descriptions (IC Rev. 1.2)

Signal Name	Register	Bit	Description	Hardwired Setting
SDQS3	sw_pad_ctl_sdqs3_nfwe_b_nfre	21	Register bit “dse0” shows value of 0, but is overridden per Hardwired Setting column.	Drive strength set to high drive; cannot be configured for nominal or max drive.
SDQS2	sw_pad_ctl_sdqs0_sdqs1_sdqs2	1	Register bit “dse0” shows value of 0, but is overridden per Hardwired Setting column.	Drive strength set to high drive; cannot be configured for nominal or max drive.
SDQS1	sw_pad_ctl_sdqs0_sdqs1_sdqs2	11	Register bit “dse0” shows value of 0, but is overridden per Hardwired Setting column.	Drive strength set to high drive; cannot be configured for nominal or max drive.
SDQS0	sw_pad_ctl_sdqs0_sdqs1_sdqs2	21	Register bit “dse0” shows value of 0, but is overridden per Hardwired Setting column.	Drive strength set to high drive; cannot be configured for nominal or max drive.
SDBA1	sw_pad_ctl_a24_a25_sdba1	1	Register bit “dse0” shows value of 0, but is overridden per Hardwired Setting column.	Drive strength set to high drive; cannot be configured for nominal or max drive.
SDBA0	sw_pad_ctl_sdba0_sd0_sd1	21	Register bit “dse0” shows value of 0, but is overridden per Hardwired Setting column.	Drive strength set to high drive; cannot be configured for nominal or max drive.
SDCKE1	sw_pad_ctl_sdcke1_sdclk_sdclk	21	Register bit “dse0” shows value of 0, but is overridden per Hardwired Setting column.	Drive strength set to high drive; cannot be configured for nominal or max drive.
SDCKE0	sw_pad_ctl_cas_sdwe_sdcke0	1	Register bit “dse0” shows value of 0, but is overridden per Hardwired Setting column.	Drive strength set to high drive; cannot be configured for nominal or max drive.
SDWE	sw_pad_ctl_cas_sdwe_sdcke0	11	Register bit “dse0” shows value of 0, but is overridden per Hardwired Setting column.	Drive strength set to high drive; cannot be configured for nominal or max drive.
PC_CD1_B	sw_pad_ctl_pc_cd1_b_pc_cd2_b_pc_wait	20	Register bit “sre” shows value of 0, but is overridden per Hardwired Setting column.	Slew rate set to fast, cannot be configured for slow slew rate.
PC_CD2_B	sw_pad_ctl_pc_cd1_b_pc_cd2_b_pc_wait	10	Register bit “sre” shows value of 0, but is overridden per Hardwired Setting column.	Slew rate set to fast, cannot be configured for slow slew rate.
PC_WAIT_B	sw_pad_ctl_pc_cd1_b_pc_cd2_b_pc_wait	0	Register bit “sre” shows value of 0, but is overridden per Hardwired Setting column.	Slew rate set to fast, cannot be configured for slow slew rate.
PC_READY	sw_pad_ctl_pc_ready_pc_pwron_pc_vs1	20	Register bit “sre” shows value of 0, but is overridden per Hardwired Setting column.	Slew rate set to fast, cannot be configured for slow slew rate.
PC_PWRON	sw_pad_ctl_pc_ready_pc_pwron_pc_vs1	10	Register bit “sre” shows value of 0, but is overridden per Hardwired Setting column.	Slew rate set to fast, cannot be configured for slow slew rate.
PC_VS1	sw_pad_ctl_pc_ready_pc_pwron_pc_vs1	0	Register bit “sre” shows value of 0, but is overridden per Hardwired Setting column.	Slew rate set to fast, cannot be configured for slow slew rate.
PC_RST	sw_pad_ctl_pc_rst_ioios16_pc_rw	20	Register bit “sre” shows value of 0, but is overridden per Hardwired Setting column.	Slew rate set to fast, cannot be configured for slow slew rate.
PC_RW_B	sw_pad_ctl_pc_rst_ioios16_pc_rw	0	Register bit “sre” shows value of 0, but is overridden per Hardwired Setting column.	Slew rate set to fast, cannot be configured for slow slew rate.
PC_POE	sw_pad_ctl_pc_poe_m_request_m_grant	20	Register bit “sre” shows value of 0, but is overridden per Hardwired Setting column.	Slew rate set to fast, cannot be configured for slow slew rate.
COMPARE	sw_pad_ctl_capture_compare_watchdog_rst	11	Register bit “dse0” shows value of 0, but is overridden per Hardwired Setting column.	Drive strength set to high drive; cannot be configured for nominal or max drive.
CAPTURE	sw_pad_ctl_capture_compare_watchdog_rst	21	Register bit “dse0” shows value of 0, but is overridden per Hardwired Setting column.	Drive strength set to high drive; cannot be configured for nominal or max drive.

4.4.2 Table Headings

The headings for Table 4-12 on page 119 are defined as follows:

Package Contact Name	Lists the name assigned to the BGA ball. The ball map and signal listing are in the data sheet.
Supply	Specifies the power supply associated with the I/O signal.
Value After Reset	After the reset sequence is completed, specifies the direction of the signal and logic state.
I/O Type	Indicates the configuration of the output driver which determines the DC and AC characteristics. Data sheet DC Electrical Parameters table for GPIO is applicable when “regular” is listed. Data sheet DC Electrical Parameters table for DDR is applicable when DDR is listed. AC parameters are also in the data sheet.
Slew Rate	Indicates the output transition time capability of the output. If the signal is an input, ignore this column. The terms slow and fast are found in the data sheet DC Electrical Parameters and AC Electrical Characteristics tables.
Loopback	A connection that sends an output signal to the module’s input. The loopback feature allows the input buffer and output buffer to be enabled simultaneously. Note that most signal lines indicate No, which means there is no loopback capability.
Drive Strength	Output driver’s current source and sink capability. The terms “std”, “high”, and “max” are found in the data sheet DC Electrical Parameters table.*Pull Value and Direction* The on-chip nominal resistor value that is potentially available at each I/O. For i.MX31 and i.MX31L, the only value available is 100 kohms. Direction is either pull-up or pull-down. Note that a “pull-up” or “pull-dn” may be listed, but may be overridden by the Pull/Keeper Control column indicating “disable” which means the pull resistor is not enabled.
Pull/Keeper Control	The termination capability selected. “Pull” means pull-up/down is selected; refer to “Pull Value and Direction” column for details. “Keeper” indicates that a keeper circuit is enabled which holds a logic value without the extra current drain required by a simple pull-up/down resistor. “Disable” means there is no pull-up, pull-down, or keeper. In this case, the “Pull Value and Direction” column must be ignored.
Open Drain/Push-Pull	Specifies the output structure type. “PP” indicates push-pull which is a standard CMOS output with both active pull-up and pull-down MOSFETs. “OD” indicates open-drain which is an output with an active pull-down MOSFET but no active pull-up MOSFET.
Schmitt Trigger	Specifies whether an input has hysteresis or not. “No” indicates that an input is a standard CMOS input with no hysteresis. “Yes” indicates that a Schmitt-trigger circuit is engaged.

4.4.3 Table Subheadings

The subheadings in Table 4-12 on page 119 are defined as follows:

Control Bit(s) — Lists the associated sw_pad_ctl register bit(s). A dash in this column indicates that the default value is not controllable by software and the default cannot be overridden.

Default — Indicates the default setting after the power-up sequence is completed

Table 4-12 the i.MX31 and i.MX31L I/O settings begins on page 4-119.

Table 4-12. and i.MX31L I/O Settings

Package Contact Name	Value After Reset		Supply	I/O Type	Slew Rate		Loop back?		Drive Strength		Pull Value and Direction		Pull/Keeper Control		Open-Drain/ Push-Pull		Schmitt Trigger?	
	Direction	State			Control Bit	Default	Control Bit	Default	Control Bits	Default	Control Bits	Default	Control Bit	Default	Control Bit	Default	Control Bit	Default
Note: The following notes apply to all of the contacts described in this table: • This table represents IC revision 1.1 and 1.15. Exceptions for revision 1.2 are listed in . • IC Revision can be read on the SREV register. See IIM chapter for details. • Each unused input not specifically detailed in this table must be either (a) set up as a no connect with the associated on-chip pull-up or pull-down device enabled by software or (b) externally terminated to GND or associated positive supply directly or through a 1 kΩ resistor. • All unused outputs should be floated.																		
CAPTURE	input	pulled up	NVCC1	regular	sw_pad_ctl_capture[0]	slow	—	no	—	std	—	100k pull-up	sw_pad_ctl_capture[8]	pull	—	PP	—	no
COMPARE	input	pulled up	NVCC1	regular	sw_pad_ctl_compare[0]	slow	—	no	—	std	—	100k pull-up	—	pull	—	PP	—	no
WATCHDOG_RST	input	pulled up	NVCC1	regular	—	slow	—	no	—	std	—	100k pull-up	—	pull	—	PP	—	no
PWMO	input	floating	NVCC3	regular	sw_pad_ctl_pwmo[0]	slow	—	no	—	std	—	100k pull-up	sw_pad_ctl_pwmo[8]	disable	—	PP	sw_pad_ctl_pwmo[4]	yes
GPIO1_0	input	pulled up	NVCC1	regular	sw_pad_ctl_gpio1_0[0]	slow	—	no	sw_pad_ctl_gpio1_0[2:1]	std	—	100k pull-up	sw_pad_ctl_gpio1_0[8:7]	pull	sw_pad_ctl_gpio1_0[3]	PP	sw_pad_ctl_gpio1_0[4]	no
GPIO1_1	input	pulled up	NVCC1	regular	sw_pad_ctl_gpio1_1[0]	slow	—	no	sw_pad_ctl_gpio1_1[2:1]	std	—	100k pull-up	sw_pad_ctl_gpio1_1[8:7]	pull	sw_pad_ctl_gpio1_1[3]	PP	sw_pad_ctl_gpio1_1[4]	no
GPIO1_2	input	pulled up	NVCC1	regular	sw_pad_ctl_gpio1_2[0]	slow	—	no	sw_pad_ctl_gpio1_2[2:1]	std	—	100k pull-up	sw_pad_ctl_gpio1_2[8:7]	pull	sw_pad_ctl_gpio1_2[3]	PP	sw_pad_ctl_gpio1_2[4]	no
GPIO1_3	input	pulled up	NVCC1	regular	sw_pad_ctl_gpio1_3[0]	slow	—	no	sw_pad_ctl_gpio1_3[2:1]	std	—	100k pull-up	sw_pad_ctl_gpio1_3[8:7]	pull	sw_pad_ctl_gpio1_3[3]	PP	sw_pad_ctl_gpio1_3[4]	no

Table 4-12. and i.MX31L I/O Settings (continued)

Package Contact Name	Value After Reset		Supply	I/O Type	Slew Rate		Loop back?		Drive Strength		Pull Value and Direction		Pull/Keeper Control		Open-Drain/ Push-Pull		Schmitt Trigger?	
	Direction	State			Control Bit	Default	Control Bit	Default	Control Bits	Default	Control Bits	Default	Control Bit	Default	Control Bit	Default	Control Bit	Default
GPIO1_4	input	pulled up	NVCC1	regular	sw_pad_ctl_ gpio1_4[0]	slow	—	no	sw_pad_ ctl_gpio1 _4[2:1]	std	—	100k pull-up	sw_pad_c tl_gpio1_4 [8:7]	pull	sw_pad _ctl_gp io1_4[3]	PP	sw_pad _ctl_gpi o1_4[4]	no
GPIO1_5 **note 1**	input	pulled up	NVCC1	regular	sw_pad_ctl_ gpio1_5[0]	slow	—	no	sw_pad_ ctl_gpio1 _5[2:1]	std	—	100k pull-up	sw_pad_c tl_gpio1_5 [8:7]	pull	sw_pad _ctl_gp io1_5[3]	PP	sw_pad _ctl_gpi o1_5[4]	no
Note 1: GPIO1_5 should be connected to an external power management IC power ready output signal. If not used, GPIO1_5 must either be (a) externally pulled-up to NVCC1 or (b) a no connect, internally pulled-up by enabling the on-chip pull-up resistor. GPIO1_5 is a dedicated input and cannot be used as a general-purpose input/output.																		
GPIO1_6	input	pulled up	NVCC1	regular	sw_pad_ctl_ gpio1_6[0]	slow	—	no	sw_pad_ ctl_gpio1 _6[2:1]	std	—	100k pull-up	sw_pad_c tl_gpio1_6 [8:7]	pull	sw_pad _ctl_gp io1_6[3]	PP	sw_pad _ctl_gpi o1_6[4]	no
GPIO3_0	input	pulled up	NVCC4	regular	sw_pad_ctl_ gpio3_0[0]	slow	—	no	sw_pad_ ctl_gpio3 _0[2:1]	std	—	100k pull-up	sw_pad_c tl_gpio3_0 [8:7]	pull	sw_pad _ctl_gp io3_0[3]	PP	sw_pad _ctl_gpi o3_0[4]	no
GPIO3_1	input	pulled up	NVCC4	regular	sw_pad_ctl_ gpio3_1[0]	slow	—	no	sw_pad_ ctl_gpio3 _1[2:1]	std	—	100k pull-up	sw_pad_c tl_gpio3_1 [8:7]	pull	sw_pad _ctl_gp io3_1[3]	PP	sw_pad _ctl_gpi o3_1[4]	no
SCLK0	input	pulled up	NVCC9	regular	sw_pad_ctl_ sclk0[0]	slow	sw_pad _ctl_ sclk0[9]	no	sw_pad_ ctl_ sclk0[2:1]	std	—	100k pull-up	sw_pad_c tl_sclk0[8]	pull	—	PP	—	no
SRST0	input	pulled up	NVCC9	regular	sw_pad_ctl_sr st0[0]	slow	—	no	sw_pad_ ctl_srst0 [2:1]	std	—	100k pull-up	sw_pad_c tl_srst0[8]	pull	—	PP	—	no
SVEN0	input	pulled up	NVCC9	regular	sw_pad_ctl_s ven0[0]	slow	—	no	sw_pad_ ctl_sven0 [2:1]	std	—	100k pull-up	sw_pad_c tl_sven0[8]	pull	—	PP	—	no

Table 4-12. and i.MX31L I/O Settings (continued)

Package Contact Name	Value After Reset		Supply	I/O Type	Slew Rate		Loop back?		Drive Strength		Pull Value and Direction		Pull/Keeper Control		Open-Drain/ Push-Pull		Schmitt Trigger?	
	Direction	State			Control Bit	Default	Control Bit	Default	Control Bits	Default	Control Bits	Default	Control Bit	Default	Control Bit	Default	Control Bit	Default
STX0	input	pulled up	NVCC9	regular	sw_pad_ctl_stx0[0]	slow	sw_pad_ctl_stx0[9]	yes	sw_pad_ctl_stx0[2]	std	—	100k pull-up	sw_pad_ctl_stx0[8]	pull	—	PP	—	no
SRX0	input	pulled up	NVCC9	regular	sw_pad_ctl_srx0[0]	slow	—	no	sw_pad_ctl_srx0[2]	std	—	100k pull-up	sw_pad_ctl_srx0[8]	pull	—	PP	—	no
SIMPD0	input	pulled up	NVCC9	regular	sw_pad_ctl_simpd0[0]	slow	—	no	sw_pad_ctl_simpd0[2:1]	std	—	100k pull-up	sw_pad_ctl_simpd0[8]	pull	—	PP	—	no
CKIH	input	floating	NVCC1	regular	—	slow	—	no	—	std	—	100k pull-up	—	disable	—	PP	sw_pad_ctl_ckih[4]	yes
$\overline{\text{RESET\_IN}}$	input	pulled up	NVCC1	regular	—	slow	—	no	—	std	—	100k pull-up	—	pull	—	PP	—	yes
$\overline{\text{POR}}$	input	pulled up	NVCC1	regular	—	slow	—	no	—	std	—	100k pull-up	—	pull	—	PP	—	yes
CLKO	output	toggling	NVCC1	regular	—	fast	—	no	—	max	—	100k pull-up	—	disable	—	PP	—	no
BOOT_MODE0	input	floating	NVCC1	regular	—	slow	—	no	—	std	—	100k pull-up	—	disable	—	PP	—	no
BOOT_MODE1	input	floating	NVCC1	regular	—	slow	—	no	—	std	—	100k pull-up	—	disable	—	PP	—	no
BOOT_MODE2	input	floating	NVCC1	regular	—	slow	—	no	—	std	—	100k pull-up	—	disable	—	PP	—	no
BOOT_MODE3	input	floating	NVCC1	regular	—	slow	—	no	—	std	—	100k pull-up	—	disable	—	PP	—	no
BOOT_MODE4	input	floating	NVCC1	regular	—	slow	—	no	—	std	—	100k pull-up	—	disable	—	PP	—	no
CKIL	input	floating	NVCC1	regular	—	slow	—	no	—	std	—	100k pull-up	—	disable	—	PP	—	yes

Table 4-12. and i.MX31L I/O Settings (continued)

Package Contact Name	Value After Reset		Supply	I/O Type	Slew Rate		Loop back?		Drive Strength		Pull Value and Direction		Pull/Keeper Control		Open-Drain/ Push-Pull		Schmitt Trigger?	
	Direction	State			Control Bit	Default	Control Bit	Default	Control Bits	Default	Control Bits	Default	Control Bit	Default	Control Bit	Default	Control Bit	Default
POWER_FAIL	input	pulled down	NVCC1	regular	—	slow	—	no	—	std	—	100k pull-dn	—	pull	—	PP	—	no
VSTBY	output	low	NVCC1	regular	—	slow	—	no	—	std	—	100k pull-up	—	disable	—	PP	—	no
DVFS0	output	low	NVCC1	regular	—	slow	—	no	—	std	—	100k pull-up	—	disable	—	PP	—	no
DVFS1	output	low	NVCC1	regular	—	slow	—	no	—	std	—	100k pull-up	—	disable	—	PP	—	no
VPG0	output	low	NVCC1	regular	—	slow	—	no	—	std	—	100k pull-up	—	disable	—	PP	—	no
VPG1	output	low	NVCC1	regular	—	slow	—	no	—	std	—	100k pull-up	—	disable	—	PP	—	no
A0	output	low	NVCC22	regular	—	fast	—	no	sw_pad_ctl_a0[2]	max	—	100k pull-up	—	disable	—	PP	—	no
A1	output	low	NVCC22	regular	—	fast	—	no	sw_pad_ctl_a1[2]	max	—	100k pull-up	—	disable	—	PP	—	no
A2	output	low	NVCC22	regular	—	fast	—	no	sw_pad_ctl_a2[2]	max	—	100k pull-up	—	disable	—	PP	—	no
A3	output	low	NVCC22	regular	—	fast	—	no	sw_pad_ctl_a3[2]	max	—	100k pull-up	—	disable	—	PP	—	no
A4	output	low	NVCC22	regular	—	fast	—	no	sw_pad_ctl_a4[2]	max	—	100k pull-up	—	disable	—	PP	—	no
A5	output	low	NVCC22	regular	—	fast	—	no	sw_pad_ctl_a5[2]	max	—	100k pull-up	—	disable	—	PP	—	no
A6	output	low	NVCC22	regular	—	fast	—	no	sw_pad_ctl_a6[2]	max	—	100k pull-up	—	disable	—	PP	—	no
A7	output	low	NVCC22	regular	—	fast	—	no	sw_pad_ctl_a7[2]	max	—	100k pull-up	—	disable	—	PP	—	no

Table 4-12. and i.MX31L I/O Settings (continued)

Package Contact Name	Value After Reset		Supply	I/O Type	Slew Rate		Loop back?		Drive Strength		Pull Value and Direction		Pull/Keeper Control		Open-Drain/ Push-Pull		Schmitt Trigger?	
	Direction	State			Control Bit	Default	Control Bit	Default	Control Bits	Default	Control Bits	Default	Control Bit	Default	Control Bit	Default	Control Bit	Default
A8	output	low	NVCC22	regular	—	fast	—	no	sw_pad_ctl_a8[2]	max	—	100k pull-up	—	disable	—	PP	—	no
A9	output	low	NVCC22	regular	—	fast	—	no	sw_pad_ctl_a9[2]	max	—	100k pull-up	—	disable	—	PP	—	no
A10	output	low	NVCC2	regular	—	fast	—	no	sw_pad_ctl_a10[2]	max	—	100k pull-up	—	disable	—	PP	—	no
MA10	output	low	NVCC22	regular	—	fast	—	no	sw_pad_ctl_ma10[2]	max	—	100k pull-up	—	disable	—	PP	—	no
A11	output	low	NVCC22	regular	—	fast	—	no	sw_pad_ctl_a11[2]	max	—	100k pull-up	—	disable	—	PP	—	no
A12	output	low	NVCC22	regular	—	fast	—	no	sw_pad_ctl_a12[2]	max	—	100k pull-up	—	disable	—	PP	—	no
A13	output	low	NVCC22	regular	—	fast	—	no	sw_pad_ctl_a13[2]	max	—	100k pull-up	—	disable	—	PP	—	no
A14	output	low	NVCC21	regular	—	fast	—	no	sw_pad_ctl_a14[2]	max	—	100k pull-up	—	disable	—	PP	—	no
A15	output	low	NVCC21	regular	—	fast	—	no	sw_pad_ctl_a15[2]	max	—	100k pull-up	—	disable	—	PP	—	no
A16	output	low	NVCC21	regular	—	fast	—	no	sw_pad_ctl_a16[2]	max	—	100k pull-up	—	disable	—	PP	—	no
A17	output	low	NVCC22	regular	—	fast	—	no	sw_pad_ctl_a17[2]	max	—	100k pull-up	—	disable	—	PP	—	no

Table 4-12. and i.MX31L I/O Settings (continued)

Package Contact Name	Value After Reset		Supply	I/O Type	Slew Rate		Loop back?		Drive Strength		Pull Value and Direction		Pull/Keeper Control		Open-Drain/ Push-Pull		Schmitt Trigger?	
	Direction	State			Control Bit	Default	Control Bit	Default	Control Bits	Default	Control Bits	Default	Control Bit	Default	Control Bit	Default	Control Bit	Default
A18	output	low	NVCC22	regular	—	fast	—	no	sw_pad_ctl_a18[2]	max	—	100k pull-up	—	disable	—	PP	—	no
A19	output	low	NVCC22	regular	—	fast	—	no	sw_pad_ctl_a19[2]	max	—	100k pull-up	—	disable	—	PP	—	no
A20	output	low	NVCC22	regular	—	fast	—	no	sw_pad_ctl_a20[2]	max	—	100k pull-up	—	disable	—	PP	—	no
A21	output	low	NVCC22	regular	—	fast	—	no	sw_pad_ctl_a21[2]	max	—	100k pull-up	—	disable	—	PP	—	no
A22	output	low	NVCC22	regular	—	fast	—	no	sw_pad_ctl_a22[2]	max	—	100k pull-up	—	disable	—	PP	—	no
A23	output	low	NVCC22	regular	—	fast	—	no	sw_pad_ctl_a23[2]	max	—	100k pull-up	—	disable	—	PP	—	no
A24	output	low	NVCC22	regular	—	fast	—	no	sw_pad_ctl_a24[2]	max	—	100k pull-up	—	disable	—	PP	—	no
A25	output	low	NVCC22	regular	—	fast	—	no	sw_pad_ctl_a25[2]	max	—	100k pull-up	—	disable	—	PP	—	no
SDBA1	output	low	NVCC22	regular	—	fast	—	no	—	std	—	100k pull-up	—	disable	—	PP	—	no
SDBA0	output	low	NVCC22	regular	—	fast	—	no	—	std	—	100k pull-up	—	disable	—	PP	—	no
SD0	input	low	NVCC21	DDR	—	fast	—	no	sw_pad_ctl_sd0[2]	max	—	100k pull-up	—	keep	—	PP	—	no

Table 4-12. and i.MX31L I/O Settings (continued)

Package Contact Name	Value After Reset		Supply	I/O Type	Slew Rate		Loop back?		Drive Strength		Pull Value and Direction		Pull/Keeper Control		Open-Drain/ Push-Pull		Schmitt Trigger?	
	Direction	State			Control Bit	Default	Control Bit	Default	Control Bits	Default	Control Bits	Default	Control Bit	Default	Control Bit	Default	Control Bit	Default
SD1	input	low	NVCC21	DDR	—	fast	—	no	sw_pad_ctl_sd1[2]	max	—	100k pull-up	—	keep	—	PP	—	no
SD2	input	low	NVCC21	DDR	—	fast	—	no	sw_pad_ctl_sd2[2]	max	—	100k pull-up	—	keep	—	PP	—	no
SD3	input	low	NVCC21	DDR	—	fast	—	no	sw_pad_ctl_sd3[2]	max	—	100k pull-up	—	keep	—	PP	—	no
SD4	input	low	NVCC21	DDR	—	fast	—	no	sw_pad_ctl_sd4[2]	max	—	100k pull-up	—	keep	—	PP	—	no
SD5	input	low	NVCC21	DDR	—	fast	—	no	sw_pad_ctl_sd5[2]	max	—	100k pull-up	—	keep	—	PP	—	no
SD6	input	low	NVCC21	DDR	—	fast	—	no	sw_pad_ctl_sd6[2]	max	—	100k pull-up	—	keep	—	PP	—	no
SD7	input	low	NVCC21	DDR	—	fast	—	no	sw_pad_ctl_sd7[2]	max	—	100k pull-up	—	keep	—	PP	—	no
SD8	input	low	NVCC21	DDR	—	fast	—	no	sw_pad_ctl_sd8[2]	max	—	100k pull-up	—	keep	—	PP	—	no
SD9	input	low	NVCC21	DDR	—	fast	—	no	sw_pad_ctl_sd9[2]	max	—	100k pull-up	—	keep	—	PP	—	no
SD10	input	low	NVCC22	DDR	—	fast	—	no	sw_pad_ctl_sd10[2]	max	—	100k pull-up	—	keep	—	PP	—	no

Table 4-12. and i.MX31L I/O Settings (continued)

Package Contact Name	Value After Reset		Supply	I/O Type	Slew Rate		Loop back?		Drive Strength		Pull Value and Direction		Pull/Keeper Control		Open-Drain/ Push-Pull		Schmitt Trigger?	
	Direction	State			Control Bit	Default	Control Bit	Default	Control Bits	Default	Control Bits	Default	Control Bit	Default	Control Bit	Default	Control Bit	Default
SD11	input	low	NVCC22	DDR	—	fast	—	no	sw_pad_ctl_sd11[2]	max	—	100k pull-up	—	keep	—	PP	—	no
SD12	input	low	NVCC22	DDR	—	fast	—	no	sw_pad_ctl_sd12[2]	max	—	100k pull-up	—	keep	—	PP	—	no
SD13	input	low	NVCC22	DDR	—	fast	—	no	sw_pad_ctl_sd13[2]	max	—	100k pull-up	—	keep	—	PP	—	no
SD14	input	low	NVCC22	DDR	—	fast	—	no	sw_pad_ctl_sd14[2]	max	—	100k pull-up	—	keep	—	PP	—	no
SD15	input	low	NVCC22	DDR	—	fast	—	no	sw_pad_ctl_sd15[2]	max	—	100k pull-up	—	keep	—	PP	—	no
SD16	input	low	NVCC22	DDR	—	fast	—	no	sw_pad_ctl_sd16[2]	max	—	100k pull-up	—	keep	—	PP	—	no
SD17	input	low	NVCC22	DDR	—	fast	—	no	sw_pad_ctl_sd17[2]	max	—	100k pull-up	—	keep	—	PP	—	no
SD18	input	low	NVCC22	DDR	—	fast	—	no	sw_pad_ctl_sd18[2]	max	—	100k pull-up	—	keep	—	PP	—	no
SD19	input	low	NVCC22	DDR	—	fast	—	no	sw_pad_ctl_sd19[2]	max	—	100k pull-up	—	keep	—	PP	—	no
SD20	input	low	NVCC22	DDR	—	fast	—	no	sw_pad_ctl_sd20[2]	max	—	100k pull-up	—	keep	—	PP	—	no

Table 4-12. and i.MX31L I/O Settings (continued)

Package Contact Name	Value After Reset		Supply	I/O Type	Slew Rate		Loop back?		Drive Strength		Pull Value and Direction		Pull/Keeper Control		Open-Drain/ Push-Pull		Schmitt Trigger?	
	Direction	State			Control Bit	Default	Control Bit	Default	Control Bits	Default	Control Bits	Default	Control Bit	Default	Control Bit	Default	Control Bit	Default
SD21	input	low	NVCC22	DDR	—	fast	—	no	sw_pad_ctl_sd21[2]	max	—	100k pull-up	—	keep	—	PP	—	no
SD22	input	low	NVCC22	DDR	—	fast	—	no	sw_pad_ctl_sd22[2]	max	—	100k pull-up	—	keep	—	PP	—	no
SD23	input	low	NVCC22	DDR	—	fast	—	no	sw_pad_ctl_sd23[2]	max	—	100k pull-up	—	keep	—	PP	—	no
SD24	input	low	NVCC22	DDR	—	fast	—	no	sw_pad_ctl_sd24[2]	max	—	100k pull-up	—	keep	—	PP	—	no
SD25	input	low	NVCC22	DDR	—	fast	—	no	sw_pad_ctl_sd25[2]	max	—	100k pull-up	—	keep	—	PP	—	no
SD26	input	low	NVCC22	DDR	—	fast	—	no	sw_pad_ctl_sd26[2]	max	—	100k pull-up	—	keep	—	PP	—	no
SD27	input	low	NVCC22	DDR	—	fast	—	no	sw_pad_ctl_sd27[2]	max	—	100k pull-up	—	keep	—	PP	—	no
SD28	input	low	NVCC22	DDR	—	fast	—	no	sw_pad_ctl_sd28[2]	max	—	100k pull-up	—	keep	—	PP	—	no
SD29	input	low	NVCC22	DDR	—	fast	—	no	sw_pad_ctl_sd29[2]	max	—	100k pull-up	—	keep	—	PP	—	no
SD30	input	low	NVCC22	DDR	—	fast	—	no	sw_pad_ctl_sd30[2]	max	—	100k pull-up	—	keep	—	PP	—	no

Table 4-12. and i.MX31L I/O Settings (continued)

Package Contact Name	Value After Reset		Supply	I/O Type	Slew Rate		Loop back?		Drive Strength		Pull Value and Direction		Pull/Keeper Control		Open-Drain/ Push-Pull		Schmitt Trigger?	
	Direction	State			Control Bit	Default	Control Bit	Default	Control Bits	Default	Control Bits	Default	Control Bit	Default	Control Bit	Default	Control Bit	Default
SD31	input	low	NVCC22	DDR	—	fast	—	no	sw_pad_ctl_sd31[2]	max	—	100k pull-up	—	keep	—	PP	—	no
DQM0	output	low	NVCC2	DDR	—	fast	—	no	sw_pad_ctl_dqm0[2]	max	—	100k pull-up	—	keep	—	PP	—	no
DQM1	output	low	NVCC2	DDR	—	fast	—	no	sw_pad_ctl_dqm1[2]	max	—	100k pull-up	—	keep	—	PP	—	no
DQM2	output	low	NVCC2	DDR	—	fast	—	no	sw_pad_ctl_dqm2[2]	max	—	100k pull-up	—	keep	—	PP	—	no
DQM3	output	low	NVCC21	DDR	—	fast	—	no	sw_pad_ctl_dqm3[2]	max	—	100k pull-up	—	keep	—	PP	—	no
EB0	output	high	NVCC2	regular	—	fast	—	no	sw_pad_ctl_eb0[2]	high	—	100k pull-up	—	disable	—	PP	—	no
EB1	output	high	NVCC2	regular	—	fast	—	no	sw_pad_ctl_eb1[2]	high	—	100k pull-up	—	disable	—	PP	—	no
OE	output	high	NVCC2	regular	—	fast	—	no	sw_pad_ctl_oe[2]	high	—	100k pull-up	—	disable	—	PP	—	no
CS0	output	high	NVCC2	regular	—	fast	—	no	sw_pad_ctl_cs0[2]	high	—	100k pull-up	—	disable	—	PP	—	no
CS1	output	high	NVCC2	regular	—	fast	—	no	sw_pad_ctl_cs1[2]	high	—	100k pull-up	—	disable	—	PP	—	no
CS2	output	high	NVCC2	regular	—	fast	—	no	sw_pad_ctl_cs2[2]	max	—	100k pull-up	—	keep	—	PP	—	no
CS3	output	high	NVCC2	regular	—	fast	—	no	sw_pad_ctl_cs3[2]	max	—	100k pull-up	—	keep	—	PP	—	no

Table 4-12. and i.MX31L I/O Settings (continued)

Package Contact Name	Value After Reset		Supply	I/O Type	Slew Rate		Loop back?		Drive Strength		Pull Value and Direction		Pull/Keeper Control		Open-Drain/ Push-Pull		Schmitt Trigger?	
	Direction	State			Control Bit	Default	Control Bit	Default	Control Bits	Default	Control Bits	Default	Control Bit	Default	Control Bit	Default	Control Bit	Default
CS4	output	high	NVCC2	regular	—	fast	—	no	sw_pad_ctl_cs4[2]	high	—	100k pull-up	—	disable	—	PP	—	no
CS5	output	high	NVCC2	regular	—	fast	—	no	sw_pad_ctl_cs5[2]	high	—	100k pull-up	—	disable	—	PP	—	no
ECB	input	pulled up	NVCC2	regular	—	fast	—	no	sw_pad_ctl_ecb[2]	high	—	100k pull-up	—	pull	—	PP	—	no
LBA	output	high	NVCC2	regular	—	fast	—	no	sw_pad_ctl_lba[2]	high	—	100k pull-up	—	disable	—	PP	—	no
BCLK	output	low	NVCC2	regular	—	fast	—	yes	sw_pad_ctl_bclk[2]	high	—	100k pull-up	—	disable	—	PP	—	no
RW	output	high	NVCC2	regular	—	fast	—	no	sw_pad_ctl_rw[2]	high	—	100k pull-up	—	disable	—	PP	—	no
RAS	output	high	NVCC2	regular	—	fast	—	no	sw_pad_ctl_ras[2]	max	—	100k pull-up	—	keep	—	PP	—	no
CAS	output	high	NVCC2	regular	—	fast	—	no	sw_pad_ctl_cas[2]	max	—	100k pull-up	—	keep	—	PP	—	no
SDWE	output	high	NVCC2	regular	—	fast	—	no	—	std	—	100k pull-up	—	keep	—	PP	—	no
SDCKE0	output	low	NVCC2	regular	—	fast	—	no	—	std	—	100k pull-up	—	keep	—	PP	—	no
SDCKE1	output	low	NVCC2	regular	—	fast	—	no	—	std	—	100k pull-up	—	keep	—	PP	—	no
SDCLK **note 2**	output	toggling	NVCC2	regular	—	fast	—	yes	sw_pad_ctl_sdclk[2]	max	—	100k pull-up	—	disable	—	PP	—	no

Note 2: **SDCLK** and **$\overline{\text{SDCLK}}$** is a differential output pair that is controlled by the same Drive Strength bit.

Table 4-12. and i.MX31L I/O Settings (continued)

Package Contact Name	Value After Reset		Supply	I/O Type	Slew Rate		Loop back?		Drive Strength		Pull Value and Direction		Pull/Keeper Control		Open-Drain/ Push-Pull		Schmitt Trigger?	
	Direction	State			Control Bit	Default	Control Bit	Default	Control Bits	Default	Control Bits	Default	Control Bit	Default	Control Bit	Default	Control Bit	Default
$\overline{\text{SDCLK}}$ **note 2**	output	toggling	NVCC2	regular	—	fast	—	yes	sw_pad_ctl_sdclk [2]	max	—	100k pull-up	—	disable	—	PP	—	no
SDQS0	output	low	NVCC21	DDR	—	fast	—	no	—	std	—	100k pull-dn	—	pull	—	PP	—	no
SDQS1	output	low	NVCC22	DDR	—	fast	—	no	—	std	—	100k pull-dn	—	pull	—	PP	—	no
SDQS2	output	low	NVCC22	DDR	—	fast	—	no	—	std	—	100k pull-dn	—	pull	—	PP	—	no
SDQS3	output	low	NVCC22	DDR	—	fast	—	no	—	std	—	100k pull-dn	—	pull	—	PP	—	no
$\overline{\text{NFWE}}$	output	high	NVCC10	regular	$\overline{\text{sw_pad_ctl_nfwe}}$[0]	fast	—	no	$\overline{\text{sw_pad_ctl_nfwe}}$ [2:1]	high	—	100k pull-dn	$\overline{\text{sw_pad_ctl_nfwe}}$[8]	pull	—	PP	—	no
$\overline{\text{NFRE}}$	output	high	NVCC10	regular	$\overline{\text{sw_pad_ctl_nfre}}$[0]	fast	—	no	$\overline{\text{sw_pad_ctl_nfre}}$ [2:1]	high	—	100k pull-up	$\overline{\text{sw_pad_ctl_nfre}}$[8]	pull	—	PP	—	no
NFALE	output	low	NVCC10	regular	sw_pad_ctl_nfale[0]	fast	—	no	sw_pad_ctl_nfale [2:1]	high	—	100k pull-up	sw_pad_ctl_nfale[8]	pull	—	PP	—	no
NFCLE	output	low	NVCC10	regular	sw_pad_ctl_nfcle[0]	fast	—	no	sw_pad_ctl_nfcle [2:1]	high	—	100k pull-up	sw_pad_ctl_nfcle[8]	pull	—	PP	—	no
$\overline{\text{NFWP}}$	output	low during reset/ high after reset	NVCC10	regular	$\overline{\text{sw_pad_ctl_nfwp}}$[0]	fast	—	no	$\overline{\text{sw_pad_ctl_nfwp}}$ [2:1]	high	—	100k pull-up	$\overline{\text{sw_pad_ctl_nfwp}}$[8]	pull	—	PP	—	no
$\overline{\text{NFCE}}$	output	high	NVCC10	regular	$\overline{\text{sw_pad_ctl_nfce}}$[0]	fast	—	no	$\overline{\text{sw_pad_ctl_nfce}}$ [2:1]	high	—	100k pull-up	$\overline{\text{sw_pad_ctl_nfce}}$[8]	pull	—	PP	—	no

Table 4-12. and i.MX31L I/O Settings (continued)

Package Contact Name	Value After Reset		Supply	I/O Type	Slew Rate		Loop back?		Drive Strength		Pull Value and Direction		Pull/Keeper Control		Open-Drain/ Push-Pull		Schmitt Trigger?	
	Direction	State			Control Bit	Default	Control Bit	Default	Control Bits	Default	Control Bits	Default	Control Bit	Default	Control Bit	Default	Control Bit	Default
NFRB	input	pulled up	NVCC10	regular	sw_pad_ctl_nfrb[0]	fast	—	no	sw_pad_ctl_nfrb[2:1]	high	—	100k pull-up	sw_pad_ctl_nfrb[8]	pull	—	PP	—	no
D15	input	low	NVCC10	regular	—	fast	—	no	sw_pad_ctl_d15[2]	max	—	100k pull-up	—	keep	—	PP	—	no
D14	input	low	NVCC10	regular	—	fast	—	no	sw_pad_ctl_d14[2]	max	—	100k pull-up	—	keep	—	PP	—	no
D13	input	low	NVCC10	regular	—	fast	—	no	sw_pad_ctl_d13[2]	max	—	100k pull-up	—	keep	—	PP	—	no
D12	input	low	NVCC10	regular	—	fast	—	no	sw_pad_ctl_d12[2]	max	—	100k pull-up	—	keep	—	PP	—	no
D11	input	low	NVCC10	regular	—	fast	—	no	sw_pad_ctl_d11[2]	max	—	100k pull-up	—	keep	—	PP	—	no
D10	input	low	NVCC10	regular	—	fast	—	no	sw_pad_ctl_d10[2]	max	—	100k pull-up	—	keep	—	PP	—	no
D9	input	low	NVCC10	regular	—	fast	—	no	sw_pad_ctl_d9[2]	max	—	100k pull-up	—	keep	—	PP	—	no
D8	input	low	NVCC10	regular	—	fast	—	no	sw_pad_ctl_d8[2]	max	—	100k pull-up	—	keep	—	PP	—	no
D7	input	low	NVCC10	regular	—	fast	—	no	sw_pad_ctl_d7[2]	max	—	100k pull-up	—	keep	—	PP	—	no
D6	input	low	NVCC10	regular	—	fast	—	no	sw_pad_ctl_d6[2]	max	—	100k pull-up	—	keep	—	PP	—	no
D5	input	low	NVCC10	regular	—	fast	—	no	sw_pad_ctl_d5[2]	max	—	100k pull-up	—	keep	—	PP	—	no

Table 4-12. and i.MX31L I/O Settings (continued)

Package Contact Name	Value After Reset		Supply	I/O Type	Slew Rate		Loop back?		Drive Strength		Pull Value and Direction		Pull/Keeper Control		Open-Drain/ Push-Pull		Schmitt Trigger?	
	Direction	State			Control Bit	Default	Control Bit	Default	Control Bits	Default	Control Bits	Default	Control Bit	Default	Control Bit	Default	Control Bit	Default
D4	input	low	NVCC10	regular	—	fast	—	no	sw_pad_ctl_d4[2]	max	—	100k pull-up	—	keep	—	PP	—	no
D3	input	low	NVCC10	regular	—	fast	—	no	sw_pad_ctl_d3[2]	max	—	100k pull-up	—	keep	—	PP	—	no
D2	input	low	NVCC10	regular	—	fast	—	no	sw_pad_ctl_d2[2]	max	—	100k pull-up	—	keep	—	PP	—	no
D1	input	low	NVCC10	regular	—	fast	—	no	sw_pad_ctl_d1[2]	max	—	100k pull-up	—	keep	—	PP	—	no
D0	input	low	NVCC10	regular	—	fast	—	no	sw_pad_ctl_d0[2]	max	—	100k pull-up	—	keep	—	PP	—	no
$\overline{\text{PC\_CD1}}$ **note 3**	input	pulled up	NVCC3	regular	—	slow	$\overline{\text{sw\_pad\_ctl\_pc\_cd1}}$[9]	no	—	high	—	100k pull-up	$\overline{\text{sw\_pad\_ctl\_pc\_cd1}}$[8]	pull	—	PP	$\overline{\text{sw\_pad\_ctl\_pc\_cd1}}$[4]	no
Note 3: $\overline{\text{PC\_CD1}}$ and $\overline{\text{PC\_CD2}}$ are controlled by same Pull/Keeper control bit.																		
$\overline{\text{PC\_CD2}}$ **note 3, 4**	input	pulled up	NVCC3	regular	—	slow	—	no	—	high	sw_pad_ctl_pc_vs1[8]	100k pull-up	$\overline{\text{sw\_pad\_ctl\_pc\_cd1}}$[8]	pull	—	PP	—	no
Note 4: The setting of $\overline{\text{sw\_pad\_ctl\_pc\_cd2}}$[8] does not effect bit **ipp_pke** of **PC_CD2**. This bit is used as the pull up/down (0=pull dn/1=pull up) select (ipp_pus1) for PC_PWRON.																		
$\overline{\text{PC\_WAIT}}$	input	pulled up	NVCC3	regular	—	slow	$\overline{\text{sw\_pad\_ctl\_pc\_wait}}$[9]	no	—	high	sw_pad_ctl_pc_vs1[8] **note 5**	100k pull-up	$\overline{\text{sw\_pad\_ctl\_pc\_wait}}$[8] **note 6**	pull	—	PP	—	no

Table 4-12. and i.MX31L I/O Settings (continued)

Package Contact Name	Value After Reset		Supply	I/O Type	Slew Rate		Loop back?		Drive Strength		Pull Value and Direction		Pull/Keeper Control		Open-Drain/ Push-Pull		Schmitt Trigger?	
	Direction	State			Control Bit	Default	Control Bit	Default	Control Bits	Default	Control Bits	Default	Control Bit	Default	Control Bit	Default	Control Bit	Default
PC_READY	input	pulled up	NVCC3	regular	—	slow	sw_pad_ctl_pc_ready [9]	no	—	high	sw_pad_ctl_pc_vs1[8] **note 5**	100k pull-up	sw_pad_ctl_pc_ready [8]	pull	—	PP	—	no
PC_PWRON	input	pulled down	NVCC3	regular	—	slow	sw_pad_ctl_pc_pwron [9]	no	—	high	sw_pad_ctl_pc_cd2[8] **note 4**	100k pull-dn	sw_pad_ctl_pc_pwron [8]	pull	—	PP	—	no
PC_VS1	input	pulled up	NVCC3	regular	—	slow	sw_pad_ctl_pc_vs1 [9]	no	—	high	sw_pad_ctl_pc_VS1[8] **note 5**	100k pull-up	$\overline{\text{sw\_pad\_ctl\_pc\_wait}}$ [8] **note 6**	pull	—	PP	—	no
Note 5: The setting of bit 8 does not effect bit **ipp_pke** of **PC_VS1**. This bit is used as the pull up/down (0=pull dn/1=pull up) select (ipp_pus1) for $\overline{\text{PC\_WAIT}}$, PC_READY, PC_VS1																		
Note 6: PC_WAIT and PC_VS1 are controlled by the same Pull/Keeper control bit.																		
PC_VS2	input	pulled up	NVCC3	regular	—	slow	—	no	—	high	—	100k pull-up	sw_pad_ctl_pc_vs2[8]	pull	—	PP	—	no
PC_BVD1	input	pulled up	NVCC3	regular	—	slow	—	no	—	high	—	100k pull-up	sw_pad_ctl_pc_bvd1 [8]	pull	—	PP	—	no
PC_BVD2	input	pulled up	NVCC3	regular	—	slow	—	no	—	high	—	100k pull-up	sw_pad_ctl_pc_bvd2 [8]	pull	—	PP	—	no

Table 4-12. and i.MX31L I/O Settings (continued)

Package Contact Name	Value After Reset		Supply	I/O Type	Slew Rate		Loop back?		Drive Strength		Pull Value and Direction		Pull/Keeper Control		Open-Drain/ Push-Pull		Schmitt Trigger?	
	Direction	State			Control Bit	Default	Control Bit	Default	Control Bits	Default	Control Bits	Default	Control Bit	Default	Control Bit	Default	Control Bit	Default
PC_RST	output	low	NVCC3	regular	—	slow	—	no	—	high	—	100k pull-up	sw_pad_ctl_pc_rst[8]	pull	—	PP	—	no
IOIS16	input	pulled up	NVCC3	regular	—	slow	—	no	—	high	—	100k pull-up	sw_pad_ctl_pc_iois16 [8]	pull	—	PP	—	no
$\overline{\text{PC\_RW}}$	output	high	NVCC3	regular	—	slow	—	no	—	high	—	100k pull-up	$\overline{\text{sw\_pad\_ctl\_pc\_rw}}$[8]	pull	—	PP	—	no
PC_POE	output	high	NVCC3	regular	—	slow	—	no	—	high	—	100k pull-up	—	disable	—	PP	—	no
M_REQUEST **note 7**	output	low	NVCC2	regular	—	slow	—	no	—	std	—	100k pull-up	—	disable	—	PP	—	no
Note 7: M_REQUEST and M_GRANT are not utilized in MX31/31L. No connections should be made to these signals.																		
M_GRANT **note 7**	input	pulled up	NVCC2	regular	—	slow	—	no	—	std	—	100k pull-up	—	pull	—	PP	—	no
CSI_D4	input	not floating	NVCC4	regular	sw_pad_ctl_csi_d4[0]	fast	—	no	sw_pad_ctl_csi_d4[2:1]	high	—	100k pull-up	sw_pad_ctl_csi_d4 [7:8]	keep	—	PP	—	no
CSI_D5	input	not floating	NVCC4	regular	sw_pad_ctl_csi_d5[0]	fast	—	no	sw_pad_ctl_csi_d5[2:1]	high	—	100k pull-up	sw_pad_ctl_csi_d5 [7:8]	keep	—	PP	—	no
CSI_D6	input	not floating	NVCC4	regular	sw_pad_ctl_csi_d6[0]	fast	—	no	sw_pad_ctl_csi_d6[2:1]	high	—	100k pull-up	sw_pad_ctl_csi_d6 [7:8]	keep	—	PP	—	no
CSI_D7	input	not floating	NVCC4	regular	sw_pad_ctl_csi_d7[0]	fast	—	no	sw_pad_ctl_csi_d7[2:1]	high	—	100k pull-up	sw_pad_ctl_csi_d7 [7:8]	keep	—	PP	—	no

Table 4-12. and i.MX31L I/O Settings (continued)

Package Contact Name	Value After Reset		Supply	I/O Type	Slew Rate		Loop back?		Drive Strength		Pull Value and Direction		Pull/Keeper Control		Open-Drain/ Push-Pull		Schmitt Trigger?	
	Direction	State			Control Bit	Default	Control Bit	Default	Control Bits	Default	Control Bits	Default	Control Bit	Default	Control Bit	Default	Control Bit	Default
CSI_D8	input	not floating	NVCC4	regular	sw_pad_ctl_csi_d8[0]	fast	—	no	sw_pad_ctl_csi_d8[2:1]	high	—	100k pull-up	sw_pad_ctl_csi_d8[7:8]	keep	—	PP	—	no
CSI_D9	input	not floating	NVCC4	regular	sw_pad_ctl_csi_d9[0]	fast	—	no	sw_pad_ctl_csi_d9[2:1]	high	—	100k pull-up	sw_pad_ctl_csi_d9[7:8]	keep	—	PP	—	no
CSI_D10	input	not floating	NVCC4	regular	sw_pad_ctl_csi_d10[0]	fast	—	no	sw_pad_ctl_csi_d10[2:1]	high	—	100k pull-up	sw_pad_ctl_csi_d10[7:8]	keep	—	PP	—	no
CSI_D11	input	not floating	NVCC4	regular	sw_pad_ctl_csi_d11[0]	fast	—	no	sw_pad_ctl_csi_d11[2:1]	high	—	100k pull-up	sw_pad_ctl_csi_d11[7:8]	keep	—	PP	—	no
CSI_D12	input	not floating	NVCC4	regular	sw_pad_ctl_csi_d12[0]	fast	—	no	sw_pad_ctl_csi_d12[2:1]	high	—	100k pull-up	sw_pad_ctl_csi_d12[7:8]	keep	—	PP	—	no
CSI_D13	input	not floating	NVCC4	regular	sw_pad_ctl_csi_d13[0]	fast	—	no	sw_pad_ctl_csi_d13[2:1]	high	—	100k pull-up	sw_pad_ctl_csi_d13[7:8]	keep	—	PP	—	no
CSI_D14	input	not floating	NVCC4	regular	sw_pad_ctl_csi_d14[0]	fast	—	no	sw_pad_ctl_csi_d14[2:1]	high	—	100k pull-up	sw_pad_ctl_csi_d14[7:8]	keep	—	PP	—	no
CSI_D15	input	not floating	NVCC4	regular	sw_pad_ctl_csi_d15[0]	fast	—	no	sw_pad_ctl_csi_d15[2:1]	high	—	100k pull-up	sw_pad_ctl_csi_d15[7:8]	keep	—	PP	—	no
CSI_MCLK	input	not floating	NVCC4	regular	sw_pad_ctl_csi_mclk[0]	fast	—	no	sw_pad_ctl_csi_mclk[2:1]	high	—	100k pull-up	sw_pad_ctl_csi_mclk[7:8]	keep	—	PP	—	no
CSI_VSYNC	input	not floating	NVCC4	regular	sw_pad_ctl_csi_vsync[0]	fast	—	no	sw_pad_ctl_csi_vsync[2:1]	high	—	100k pull-up	sw_pad_ctl_csi_vsync[7:8]	keep	—	PP	—	no

Table 4-12. and i.MX31L I/O Settings (continued)

Package Contact Name	Value After Reset		Supply	I/O Type	Slew Rate		Loop back?		Drive Strength		Pull Value and Direction		Pull/Keeper Control		Open-Drain/ Push-Pull		Schmitt Trigger?	
	Direction	State			Control Bit	Default	Control Bit	Default	Control Bits	Default	Control Bits	Default	Control Bit	Default	Control Bit	Default	Control Bit	Default
CSI_HSYNC	input	not floating	NVCC4	regular	sw_pad_ctl_csi_hsync[0]	fast	—	no	sw_pad_ctl_csi_hsync[2:1]	high	—	100k pull-up	sw_pad_ctl_csi_hsync[7:8]	keep	—	PP	—	no
CSI_PIXCLK	input	not floating	NVCC4	regular	sw_pad_ctl_csi_pixclk[0]	fast	—	no	sw_pad_ctl_csi_pixclk[2:1]	high	—	100k pull-up	sw_pad_ctl_csi_pixclk [7:8]	keep	—	PP	sw_pad_ctl_csi_pixclk[4]	yes
I2C_CLK	input	pulled up	NVCC4	regular	sw_pad_ctl_i2c_clk[0]	slow	—	no	sw_pad_ctl_i2c_clk[2:1]	std	—	100k pull-up	sw_pad_ctl_i2c_clk [8]	pull	sw_pad_ctl_i2c_clk [3]	PP	sw_pad_ctl_i2c_clk [4]	yes
I2C_DAT	input	pulled up	NVCC4	regular	sw_pad_ctl_i2c_dat[0]	slow	—	no	sw_pad_ctl_i2c_dat[2:1]	std	—	100k pull-up	sw_pad_ctl_i2c_dat[8]	pull	sw_pad_ctl_i2c_dat[3]	PP	—	yes
STXD3	input	pulled up	NVCC10	regular	sw_pad_ctl_stxd3[0]	slow	—	no	sw_pad_ctl_stxd3[2:1]	std	—	100k pull-up	sw_pad_ctl_stxd3[8]	pull	—	PP	—	no
SRXD3	input	pulled up	NVCC10	regular	sw_pad_ctl_srxd3[0]	slow	—	no	sw_pad_ctl_srxd3 [2:1]	std	—	100k pull-up	sw_pad_ctl_srxd3[8]	pull	—	PP	—	no
SCK3	input	pulled up	NVCC10	regular	sw_pad_ctl_sck3[0]	slow	—	no	sw_pad_ctl_sck3 [2:1]	std	—	100k pull-up	sw_pad_ctl_sck3[8]	pull	—	PP	sw_pad_ctl_sck3[4]	yes
SFS3	input	pulled up	NVCC10	regular	sw_pad_ctl_sfs3[0]	slow	—	no	sw_pad_ctl_sfs3 [2:1]	std	—	100k pull-up	sw_pad_ctl_sfs3[8]	pull	—	PP	—	no
STXD4	input	pulled up	NVCC5	regular	sw_pad_ctl_stxd4[0]	slow	—	no	sw_pad_ctl_stxd4 [2:1]	std	—	100k pull-up	sw_pad_ctl_stxd4[8]	pull	—	PP	—	no
SRXD4	input	pulled up	NVCC5	regular	sw_pad_ctl_srxd4[0]	slow	—	no	sw_pad_ctl_srxd4 [2:1]	std	—	100k pull-up	sw_pad_ctl_srxd4[8]	pull	—	PP	sw_pad_ctl_srxd4[4]	no

Table 4-12. and i.MX31L I/O Settings (continued)

Package Contact Name	Value After Reset		Supply	I/O Type	Slew Rate		Loop back?		Drive Strength		Pull Value and Direction		Pull/Keeper Control		Open-Drain/ Push-Pull		Schmitt Trigger?	
	Direction	State			Control Bit	Default	Control Bit	Default	Control Bits	Default	Control Bits	Default	Control Bit	Default	Control Bit	Default	Control Bit	Default
SCK4	input	pulled up	NVCC5	regular	sw_pad_ctl_sck4[0]	slow	—	no	sw_pad_ctl_sck4 [2:1]	std	—	100k pull-up	sw_pad_ctl_sck4[8]	pull	—	PP	sw_pad_ctl_sck4[4]	yes
SFS4	input	pulled up	NVCC5	regular	sw_pad_ctl_sfs4[0]	slow	—	no	sw_pad_ctl_sfs4 [2:1]	std	—	100k pull-up	sw_pad_ctl_sfs4[8]	pull	—	PP	sw_pad_ctl_sfs4[4]	no
STXD5	input	pulled up	NVCC5	regular	sw_pad_ctl_stxd5[0]	slow	—	no	sw_pad_ctl_stxd5 [2:1]	std	—	100k pull-up	sw_pad_ctl_stxd5[8]	pull	—	PP	—	no
SRXD5	input	pulled up	NVCC5	regular	sw_pad_ctl_srxd5[0]	slow	—	no	sw_pad_ctl_srxd5 [2:1]	std	—	100k pull-up	sw_pad_ctl_srxd5[8]	pull	—	PP	—	no
SCK5	input	pulled up	NVCC5	regular	sw_pad_ctl_sck5[0]	slow	—	no	sw_pad_ctl_sck5 [2:1]	std	—	100k pull-up	sw_pad_ctl_sck5[8]	pull	—	PP	sw_pad_ctl_sck5[4]	yes
SFS5	input	pulled up	NVCC5	regular	sw_pad_ctl_sfs5[0]	slow	—	no	sw_pad_ctl_sfs5 [2:1]	std	—	100k pull-up	sw_pad_ctl_sfs5[8]	pull	—	PP	—	no
STXD6	input	pulled up	NVCC10	regular	sw_pad_ctl_stxd6[0]	slow	—	no	sw_pad_ctl_stxd6 [2:1]	std	—	100k pull-up	sw_pad_ctl_stxd6[8]	pull	—	PP	—	no
SRXD6	input	pulled up	NVCC10	regular	sw_pad_ctl_srxd6[0]	slow	—	no	sw_pad_ctl_srxd6 [2:1]	std	—	100k pull-up	sw_pad_ctl_srxd6[8]	pull	—	PP	—	no
SCK6	input	pulled up	NVCC10	regular	sw_pad_ctl_sck6[0]	slow	—	no	sw_pad_ctl_sck6 [2:1]	std	—	100k pull-up	sw_pad_ctl_sck6[8]	pull	—	PP	sw_pad_ctl_sck6[4]	yes
SFS6	input	pulled up	NVCC10	regular	sw_pad_ctl_sfs6[0]	slow	—	no	sw_pad_ctl_sfs6 [2:1]	std	—	100k pull-up	sw_pad_ctl_sfs6[8]	pull	—	PP	—	no

Table 4-12. and i.MX31L I/O Settings (continued)

Package Contact Name	Value After Reset		Supply	I/O Type	Slew Rate		Loop back?		Drive Strength		Pull Value and Direction		Pull/Keeper Control		Open-Drain/ Push-Pull		Schmitt Trigger?	
	Direction	State			Control Bit	Default	Control Bit	Default	Control Bits	Default	Control Bits	Default	Control Bit	Default	Control Bit	Default	Control Bit	Default
CSPI1_MOSI	input	pulled up	NVCC10	regular	sw_pad_ctl_cspi1_mosi[0]	slow	—	no	sw_pad_ctl_cspi1_mosi [2:1]	std	—	100k pull-up	sw_pad_ctl_cspi1_mosi[8]	pull	—	PP	—	no
CSPI1_MISO	input	pulled up	NVCC10	regular	sw_pad_ctl_cspi1_miso[0]	slow	—	no	sw_pad_ctl_cspi1_miso [2:1]	std	—	100k pull-up	sw_pad_ctl_cspi1_miso[8]	pull	—	PP	—	no
CSPI1_SS0	input	pulled up	NVCC10	regular	sw_pad_ctl_cspi1_ss0[0]	slow	—	no	sw_pad_ctl_cspi1_ss0[2:1]	std	—	100k pull-up	sw_pad_ctl_cspi1_ss0[8]	pull	—	PP	—	no
CSPI1_SS1	input	pulled up	NVCC10	regular	sw_pad_ctl_cspi1_ss1[0]	slow	—	no	sw_pad_ctl_cspi1_ss1[2:1]	std	—	100k pull-up	sw_pad_ctl_cspi1_ss1[8]	pull	—	PP	—	no
CSPI1_SS2	input	pulled up	NVCC10	regular	sw_pad_ctl_cspi1_ss2[0]	slow	—	no	sw_pad_ctl_cspi1_ss2[2:1]	std	—	100k pull-up	sw_pad_ctl_cspi1_ss2[8]	pull	—	PP	—	no
CSPI1_SCLK	input	pulled up	NVCC10	regular	sw_pad_ctl_cspi1_sclk[0]	slow	—	no	sw_pad_ctl_cspi1_sclk[2:1]	std	—	100k pull-up	sw_pad_ctl_cspi1_sclk[8]	pull	—	PP	sw_pad_ctl_cspi1_sclk[4]	yes
CSPI1_SPI_RDY	input	pulled up	NVCC10	regular	sw_pad_ctl_cspi1_spi_rdy[0]	slow	—	no	sw_pad_ctl_cspi1_spi_rdy[2:1]	std	—	100k pull-up	sw_pad_ctl_cspi1_spi_rdy[8]	pull	—	PP	—	no
CSPI2_MOSI	input	pulled up	NVCC5	regular	sw_pad_ctl_cspi2_mosi[0]	slow	—	no	sw_pad_ctl_cspi2_mosi[2:1]	std	—	100k pull-up	sw_pad_ctl_cspi2_mosi[8]	pull	sw_pad_ctl_cspi2_mosi[3]	PP	—	yes
CSPI2_MISO	input	pulled up	NVCC5	regular	sw_pad_ctl_cspi2_miso[0]	slow	—	no	sw_pad_ctl_cspi2_miso[2:1]	std	—	100k pull-up	sw_pad_ctl_cspi2_miso[8]	pull	sw_pad_ctl_cspi2_miso[3]	PP	—	yes

Table 4-12. and i.MX31L I/O Settings (continued)

Package Contact Name	Value After Reset		Supply	I/O Type	Slew Rate		Loop back?		Drive Strength		Pull Value and Direction		Pull/Keeper Control		Open-Drain/ Push-Pull		Schmitt Trigger?	
	Direction	State			Control Bit	Default	Control Bit	Default	Control Bits	Default	Control Bits	Default	Control Bit	Default	Control Bit	Default	Control Bit	Default
CSPI2_SS0	input	pulled up	NVCC5	regular	sw_pad_ctl_cspi2_ss0[0]	slow	—	no	sw_pad_ctl_cspi2_ss0[2:1]	std	—	100k pull-up	sw_pad_ctl_cspi2_ss0[8]	pull	—	PP	—	no
CSPI2_SS1	input	pulled up	NVCC5	regular	sw_pad_ctl_cspi2_ss1[0]	slow	—	no	sw_pad_ctl_cspi2_ss1[2:1]	std	—	100k pull-up	sw_pad_ctl_cspi2_ss1[8]	pull	—	PP	—	no
CSPI2_SS2	input	pulled up	NVCC5	regular	sw_pad_ctl_cspi2_ss2[0]	slow	—	no	sw_pad_ctl_cspi2_ss2[2:1]	std	—	100k pull-up	sw_pad_ctl_cspi2_ss2[8]	pull	sw_pad_ctl_cspi2_ss2[3]	PP	—	yes
CSPI2_SCLK	input	pulled up	NVCC5	regular	sw_pad_ctl_cspi2_sclk[0]	slow	—	no	sw_pad_ctl_cspi2_sclk[2:1]	std	—	100k pull-up	sw_pad_ctl_cspi2_sclk[8]	pull	sw_pad_ctl_cspi2_sclk[3]	PP	sw_pad_ctl_cspi2_sclk[4]	yes
CSPI2_SPI_RDY	input	pulled up	NVCC5	regular	sw_pad_ctl_cspi2_spi_rdy[0]	slow	—	no	sw_pad_ctl_cspi2_spi_rdy[2:1]	std	—	100k pull-up	sw_pad_ctl_cspi2_spi_rdy[8]	pull	—	PP	—	no
RXD1	input	pulled up	NVCC8	regular	sw_pad_ctl_rxd1[0]	slow	—	no	sw_pad_ctl_rxd1[2:1]	std	—	100k pull-up	sw_pad_ctl_rxd1[8]	pull	—	PP	—	no
TXD1	input	pulled up	NVCC8	regular	sw_pad_ctl_txd1[0]	slow	—	no	sw_pad_ctl_txd1[2:1]	std	—	100k pull-up	sw_pad_ctl_txd1[8]	pull	—	PP	sw_pad_ctl_txd1[4]	no
RTS1	input	pulled up	NVCC8	regular	sw_pad_ctl_rts1[0]	slow	—	no	sw_pad_ctl_rts1[2:1]	std	—	100k pull-up	sw_pad_ctl_rts1[8]	pull	—	PP	—	no
CTS1	input	pulled up	NVCC8	regular	sw_pad_ctl_cts1[0]	slow	—	no	sw_pad_ctl_cts1[2:1]	std	—	100k pull-up	sw_pad_ctl_cts1[8]	pull	—	PP	—	no

Table 4-12. and i.MX31L I/O Settings (continued)

Package Contact Name	Value After Reset		Supply	I/O Type	Slew Rate		Loop back?		Drive Strength		Pull Value and Direction		Pull/Keeper Control		Open-Drain/ Push-Pull		Schmitt Trigger?	
	Direction	State			Control Bit	Default	Control Bit	Default	Control Bits	Default	Control Bits	Default	Control Bit	Default	Control Bit	Default	Control Bit	Default
DTR_DCE1	input	pulled up	NVCC8	regular	sw_pad_ctl_dtr_dce1[0]	slow	—	no	sw_pad_ctl_dtr_dce1[2:1]	std	—	100k pull-up	sw_pad_ctl_dtr_dce1 [8]	pull	—	PP	—	no
DSR_DCE1	input	pulled up	NVCC8	regular	sw_pad_ctl_dsr_dce1[0]	slow	—	no	sw_pad_ctl_dsr_dce1[2:1]	std	—	100k pull-up	sw_pad_ctl_dsr_dce1 [8]	pull	—	PP	sw_pad_ctl_dsr_dce1[4]	no
RI_DCE1	input	pulled up	NVCC8	regular	sw_pad_ctl_ri_dce1[0]	slow	—	no	sw_pad_ctl_ri_dce1[2:1]	std	—	100k pull-up	sw_pad_ctl_ri_dce1[8]	pull	—	PP	—	no
DCD_DCE1	input	pulled up	NVCC8	regular	sw_pad_ctl_dcd_dce1[0]	slow	—	no	sw_pad_ctl_dcd_dce1[2:1]	std	—	100k pull-up	sw_pad_ctl_dcd_dce1[8]	pull	—	PP	—	no
DTR_DTE1	input	pulled up	NVCC8	regular	sw_pad_ctl_dtr_dte1[0]	slow	—	no	sw_pad_ctl_dtr_dte1[2:1]	std	—	100k pull-up	sw_pad_ctl_dtr_dte1[8]	pull	—	PP	—	yes
DSR_DTE1	input	pulled up	NVCC8	regular	sw_pad_ctl_dsr_dte1[0]	slow	—	no	sw_pad_ctl_dsr_dte1[2:1]	std	—	100k pull-up	sw_pad_ctl_dsr_dte1[8]	pull	—	PP	—	no
RI_DTE1	input	pulled up	NVCC8	regular	sw_pad_ctl_ri_dte1[0]	slow	—	no	sw_pad_ctl_ri_dte1[2:1]	std	—	100k pull-up	sw_pad_ctl_ri_dte1[8]	pull	sw_pad_ctl_ri_dte1[3]	PP	—	yes
DCD_DTE1	input	pulled up	NVCC8	regular	sw_pad_ctl_dcd_dte1[0]	slow	—	no	sw_pad_ctl_dcd_dte1[2:1]	std	—	100k pull-up	sw_pad_ctl_dcd_dte1[8]	pull	sw_pad_ctl_dcd_dte1[3]	PP	—	no
DTR_DCE2	input	pulled up	NVCC8	regular	sw_pad_ctl_dtr_dce2[0]	slow	—	no	sw_pad_ctl_dtr_dce2[2:1]	std	—	100k pull-up	sw_pad_ctl_dtr_dce2[8]	pull	—	PP	—	no

Table 4-12. and i.MX31L I/O Settings (continued)

Package Contact Name	Value After Reset		Supply	I/O Type	Slew Rate		Loop back?		Drive Strength		Pull Value and Direction		Pull/Keeper Control		Open-Drain/ Push-Pull		Schmitt Trigger?	
	Direction	State			Control Bit	Default	Control Bit	Default	Control Bits	Default	Control Bits	Default	Control Bit	Default	Control Bit	Default	Control Bit	Default
RXD2	input	pulled up	NVCC8	regular	sw_pad_ctl_rxd2[0]	slow	—	no	sw_pad_ctl_rxd2[2:1]	std	—	100k pull-up	sw_pad_ctl_rxd2[8]	pull	—	PP	—	no
TXD2	input	pulled up	NVCC8	regular	sw_pad_ctl_txd2[0]	slow	—	no	sw_pad_ctl_txd2[2:1]	std	—	100k pull-up	sw_pad_ctl_txd2[8]	pull	—	PP	—	no
RTS2	input	pulled up	NVCC8	regular	sw_pad_ctl_rts2[0]	slow	—	no	sw_pad_ctl_rts2[2:1]	std	—	100k pull-up	sw_pad_ctl_rts2[8]	pull	—	PP	—	no
CTS2	input	pulled up	NVCC8	regular	sw_pad_ctl_cts2[0]	slow	—	no	sw_pad_ctl_cts2[2:1]	std	—	100k pull-up	sw_pad_ctl_cts2[8]	pull	—	PP	—	no
BATT_LINE	input	pulled up	NVCC5	regular	—	slow	—	yes	—	std	—	100k pull-up	sw_pad_ctl_batt_line[8]	pull	—	OD	—	no
KEY_ROW0	input	pulled up	NVCC6	regular	sw_pad_ctl_key_row0[0]	slow	—	no	—	std	—	100k pull-up	sw_pad_ctl_key_row0[8]	pull	—	PP	—	no
KEY_ROW1	input	pulled up	NVCC6	regular	sw_pad_ctl_key_row1[0]	slow	—	no	sw_pad_ctl_key_row1[2:1]	std	—	100k pull-up	sw_pad_ctl_key_row1[8]	pull	—	PP	—	no
KEY_ROW2	input	pulled up	NVCC6	regular	sw_pad_ctl_key_row2[0]	slow	—	no	sw_pad_ctl_key_row2[2:1]	std	—	100k pull-up	sw_pad_ctl_key_row2[8]	pull	—	PP	—	no
KEY_ROW3	input	pulled up	NVCC6	regular	sw_pad_ctl_key_row3[0]	slow	—	no	sw_pad_ctl_key_row3[2:1]	std	—	100k pull-up	sw_pad_ctl_key_row3[8]	pull	—	PP	—	no
KEY_ROW4	input	pulled up	NVCC6	regular	sw_pad_ctl_key_row4[0]	slow	—	no	sw_pad_ctl_key_row4[2:1]	std	—	100k pull-up	sw_pad_ctl_key_row4[8]	pull	—	PP	—	no

Table 4-12. and i.MX31L I/O Settings (continued)

Package Contact Name	Value After Reset		Supply	I/O Type	Slew Rate		Loop back?		Drive Strength		Pull Value and Direction		Pull/Keeper Control		Open-Drain/ Push-Pull		Schmitt Trigger?	
	Direction	State			Control Bit	Default	Control Bit	Default	Control Bits	Default	Control Bits	Default	Control Bit	Default	Control Bit	Default	Control Bit	Default
KEY_ROW5	input	pulled up	NVCC6	regular	sw_pad_ctl_key_row5[0]	slow	—	no	sw_pad_ctl_key_row5[2:1]	std	—	100k pull-up	sw_pad_ctl_key_row5[8]	pull	—	PP	—	no
KEY_ROW6	input	pulled up	NVCC6	regular	sw_pad_ctl_key_row6[0]	slow	—	no	sw_pad_ctl_key_row6[2:1]	std	—	100k pull-up	sw_pad_ctl_key_row6[8]	pull	—	PP	—	no
KEY_ROW7	input	pulled up	NVCC6	regular	sw_pad_ctl_key_row7[0]	slow	—	no	sw_pad_ctl_key_row7[2:1]	std	—	100k pull-up	sw_pad_ctl_key_row7[8]	pull	—	PP	—	no
KEY_COL0	input	pulled up	NVCC6	regular	sw_pad_ctl_key_col0[0]	slow	—	no	sw_pad_ctl_key_col0[2:1]	std	—	100k pull-up	sw_pad_ctl_key_col0[8]	pull	sw_pad_ctl_key_col0[3]	PP	—	no
KEY_COL1	input	pulled up	NVCC6	regular	sw_pad_ctl_key_col1[0]	slow	—	no	sw_pad_ctl_key_col1[2:1]	std	—	100k pull-up	sw_pad_ctl_key_col1[8]	pull	sw_pad_ctl_key_col1[3]	PP	—	no
KEY_COL2	input	pulled up	NVCC6	regular	sw_pad_ctl_key_col2[0]	slow	—	no	sw_pad_ctl_key_col2[2:1]	std	—	100k pull-up	sw_pad_ctl_key_col2[8]	pull	sw_pad_ctl_key_col2[3]	PP	—	no
KEY_COL3	input	pulled up	NVCC6	regular	sw_pad_ctl_key_col3[0]	slow	—	no	sw_pad_ctl_key_col3[2:1]	std	—	100k pull-up	sw_pad_ctl_key_col3[8]	pull	sw_pad_ctl_key_col3[3]	PP	—	no
KEY_COL4	input	pulled up	NVCC6	regular	sw_pad_ctl_key_col4[0]	slow	—	no	sw_pad_ctl_key_col4[2:1]	std	—	100k pull-up	sw_pad_ctl_key_col4[8]	pull	sw_pad_ctl_key_col4[3]	PP	—	no
KEY_COL5	input	pulled up	NVCC6	regular	sw_pad_ctl_key_col5[0]	slow	—	no	sw_pad_ctl_key_col5[2:1]	std	—	100k pull-up	sw_pad_ctl_key_col5[8]	pull	sw_pad_ctl_key_col5[3]	PP	—	no

Table 4-12. and i.MX31L I/O Settings (continued)

Package Contact Name	Value After Reset		Supply	I/O Type	Slew Rate		Loop back?		Drive Strength		Pull Value and Direction		Pull/Keeper Control		Open-Drain/ Push-Pull		Schmitt Trigger?	
	Direction	State			Control Bit	Default	Control Bit	Default	Control Bits	Default	Control Bits	Default	Control Bit	Default	Control Bit	Default	Control Bit	Default
KEY_COL6	input	pulled up	NVCC6	regular	sw_pad_ctl_key_col6[0]	slow	—	no	sw_pad_ctl_key_col6[2:1]	std	—	100k pull-up	sw_pad_ctl_key_col6[8]	pull	sw_pad_ctl_key_col6[3]	PP	—	no
KEY_COL7	input	pulled up	NVCC6	regular	sw_pad_ctl_key_col7[0]	slow	—	no	sw_pad_ctl_key_col7[2:1]	std	—	100k pull-up	sw_pad_ctl_key_col7[8]	pull	sw_pad_ctl_key_col7[3]	PP	—	no
RTCK	output	—	NVCC6	regular	—	fast	—	no	—	high	—	100k pull-dn	—	disable	—	PP	—	no
TCK	input	pulled down	NVCC6	regular	—	slow	—	no	—	std	—	100k pull-dn	—	pull	—	PP	—	yes
TMS	input	pulled up	NVCC6	regular	—	slow	—	no	—	std	—	100k pull-up	—	pull	—	PP	—	yes
TDI	input	pulled up	NVCC6	regular	—	slow	—	no	—	std	—	100k pull-up	—	pull	—	PP	—	yes
TDO	—	—	NVCC6	regular	—	fast	—	no	—	high	—	100k pull-up	—	disable	—	PP	—	no
TRSTB	input	pulled up	NVCC6	regular	—	slow	—	no	—	std	—	100k pull-up	—	pull	—	PP	—	no
DE_B	—	—	NVCC6	regular	—	slow	—	no	—	std	—	100k pull-up	—	pull	—	PP	—	no
SJC_MOD **note 8**	input	pulled up	NVCC6	regular	sw_pad_ctl_sjc_mod[0]	slow	—	no	sw_pad_ctl_sjc_mod[2:1]	std	—	100k pull-up	—	pull	—	PP	—	no
Note 8: SJC_MOD must be externally connected to GND for normal operation. Termination to GND through an external pull-down resistor (such as 1 kΩ) is allowed, but the value should be much smaller than the on-chip pull-up.																		
USB_PWR	input	pulled up	NVCC5	regular	sw_pad_ctl_usb_pwr[0]	slow	—	no	sw_pad_ctl_usb_pwr[2:1]	std	—	100k pull-up	sw_pad_ctl_usb_pwr[8]	pull	—	PP	—	no

Table 4-12. and i.MX31L I/O Settings (continued)

Package Contact Name	Value After Reset		Supply	I/O Type	Slew Rate		Loop back?		Drive Strength		Pull Value and Direction		Pull/Keeper Control		Open-Drain/ Push-Pull		Schmitt Trigger?	
	Direction	State			Control Bit	Default	Control Bit	Default	Control Bits	Default	Control Bits	Default	Control Bit	Default	Control Bit	Default	Control Bit	Default
USB_OC	input	pulled up	NVCC5	regular	sw_pad_ctl_usb_oc[0]	slow	—	no	sw_pad_ctl_usb_oc[2:1]	std	—	100k pull-up	sw_pad_ctl_usb_oc[8]	pull	—	PP	—	no
USB_BYP	input	pulled up	NVCC5	regular	sw_pad_ctl_usb_byp[0]	slow	—	no	sw_pad_ctl_usb_byp[2:1]	std	—	100k pull-up	sw_pad_ctl_usb_byp [8]	pull	—	PP	—	no
USBOTG_CLK	input	pulled up	NVCC5	regular	sw_pad_ctl_usbotg_clk[0]	slow	—	no	sw_pad_ctl_usbotg_clk[2:1]	std	—	100k pull-up	sw_pad_ctl_usbotg_clk[8]	pull	—	PP	sw_pad_ctl_usbotg_clk[4]	yes
USBOTG_DIR	input	pulled up	NVCC5	regular	sw_pad_ctl_usbotg_dir[0]	slow	—	no	sw_pad_ctl_usbotg_dir[2:1]	std	—	100k pull-up	sw_pad_ctl_usbotg_dir[8]	pull	—	PP	—	no
USBOTG_STP	input	pulled up	NVCC5	regular	sw_pad_ctl_usbotg_stp[0]	slow	—	no	sw_pad_ctl_usbotg_stp[2:1]	std	—	100k pull-up	sw_pad_ctl_usbotg_stp[8]	pull	—	PP	—	no
USBOTG_NXT	input	pulled up	NVCC5	regular	sw_pad_ctl_usbotg_nxt[0]	slow	—	no	sw_pad_ctl_usbotg_nxt[2:1]	std	—	100k pull-up	sw_pad_ctl_usbotg_nxt[8]	pull	—	PP	—	no
USBOTG_DATA0	input	pulled up	NVCC5	regular	sw_pad_ctl_usbotg_data0[0]	slow	—	no	sw_pad_ctl_usbotg_data0[2:1]	std	—	100k pull-up	sw_pad_ctl_usbotg_data0[8]	pull	—	PP	—	no
USBOTG_DATA1	input	pulled up	NVCC5	regular	sw_pad_ctl_usbotg_data1[0]	slow	—	no	sw_pad_ctl_usbotg_data1[2:1]	std	—	100k pull-up	sw_pad_ctl_usbotg_data1[8]	pull	—	PP	—	no
USBOTG_DATA2	input	pulled up	NVCC5	regular	sw_pad_ctl_usbotg_data2[0]	slow	—	no	sw_pad_ctl_usbotg_data2[2:1]	std	—	100k pull-up	sw_pad_ctl_usbotg_data2[8]	pull	—	PP	—	no

Table 4-12. and i.MX31L I/O Settings (continued)

Package Contact Name	Value After Reset		Supply	I/O Type	Slew Rate		Loop back?		Drive Strength		Pull Value and Direction		Pull/Keeper Control		Open-Drain/ Push-Pull		Schmitt Trigger?	
	Direction	State			Control Bit	Default	Control Bit	Default	Control Bits	Default	Control Bits	Default	Control Bit	Default	Control Bit	Default	Control Bit	Default
USBOTG_DATA3	input	pulled up	NVCC5	regular	sw_pad_ctl_usbotg_data3[0]	slow	—	no	sw_pad_ctl_usbotg_data3[2:1]	std	—	100k pull-up	sw_pad_ctl_usbotg_data3[8]	pull	—	PP	—	no
USBOTG_DATA4	input	pulled up	NVCC5	regular	sw_pad_ctl_usbotg_data4[0]	slow	—	no	sw_pad_ctl_usbotg_data4[2:1]	std	—	100k pull-up	sw_pad_ctl_usbotg_data4[8]	pull	—	PP	—	no
USBOTG_DATA5	input	pulled up	NVCC5	regular	sw_pad_ctl_usbotg_data5[0]	slow	—	no	sw_pad_ctl_usbotg_data5[2:1]	std	—	100k pull-up	sw_pad_ctl_usbotg_data5[8]	pull	—	PP	—	no
USBOTG_DATA6	input	pulled up	NVCC5	regular	sw_pad_ctl_usbotg_data6[0]	slow	—	no	sw_pad_ctl_usbotg_data6[2:1]	std	—	100k pull-up	sw_pad_ctl_usbotg_data6[8]	pull	—	PP	—	no
USBOTG_DATA7	input	pulled up	NVCC5	regular	sw_pad_ctl_usbotg_data7[0]	slow	—	no	sw_pad_ctl_usbotg_data7[2:1]	std	—	100k pull-up	sw_pad_ctl_usbotg_data7[8]	pull	—	PP	—	no
USBH2_CLK	input	pulled up	NVCC10	regular	sw_pad_ctl_usbh2_clk[0]	slow	—	no	sw_pad_ctl_usbh2_clk[2:1]	std	—	100k pull-up	sw_pad_ctl_usbh2_clk[8]	pull	—	PP	sw_pad_ctl_usbh2_clk[4]	yes
USBH2_DIR	input	pulled up	NVCC10	regular	sw_pad_ctl_usbh2_dir[0]	slow	—	no	sw_pad_ctl_usbh2_dir[2:1]	std	—	100k pull-up	sw_pad_ctl_usbh2_dir[8]	pull	—	PP	—	no
USBH2_STP	input	pulled up	NVCC10	regular	sw_pad_ctl_usbh2_stp[0]	slow	—	no	sw_pad_ctl_usbh2_stp[2:1]	std	—	100k pull-up	sw_pad_ctl_usbh2_stp[8]	pull	—	PP	—	no

Table 4-12. and i.MX31L I/O Settings (continued)

Package Contact Name	Value After Reset		Supply	I/O Type	Slew Rate		Loop back?		Drive Strength		Pull Value and Direction		Pull/Keeper Control		Open-Drain/ Push-Pull		Schmitt Trigger?	
	Direction	State			Control Bit	Default	Control Bit	Default	Control Bits	Default	Control Bits	Default	Control Bit	Default	Control Bit	Default	Control Bit	Default
USBH2_NXT	input	pulled up	NVCC10	regular	sw_pad_ctl_usbh2_nxt[0]	slow	—	no	sw_pad_ctl_usbh2_nxt[2:1]	std	—	100k pull-up	sw_pad_ctl_usbh2_nxt[8]	pull	—	PP	—	no
USBH2_DATA0	input	pulled up	NVCC10	regular	sw_pad_ctl_usbh2_data0[0]	slow	—	no	sw_pad_ctl_usbh2_data0[2:1]	std	—	100k pull-up	sw_pad_ctl_usbh2_data0[8]	pull	—	PP	—	no
USBH2_DATA1	input	pulled up	NVCC10	regular	sw_pad_ctl_usbh2_data1[0]	slow	—	no	sw_pad_ctl_usbh2_data1[2:1]	std	—	100k pull-up	sw_pad_ctl_usbh2_data1[8]	pull	—	PP	—	no
LD0	input	pulled up	NVCC7	regular	—	fast	—	no	sw_pad_ctl_ld0[2]	high	—	100k pull-up	sw_pad_ctl_ld0[7]	pull	—	PP	—	no
LD1	input	pulled up	NVCC7	regular	—	fast	—	no	sw_pad_ctl_ld1[2]	high	—	100k pull-up	sw_pad_ctl_ld1[7]	pull	—	PP	—	no
LD2	input	pulled up	NVCC7	regular	—	fast	—	no	sw_pad_ctl_ld2[2]	high	—	100k pull-up	sw_pad_ctl_ld2[7]	pull	—	PP	—	no
LD3	input	pulled up	NVCC7	regular	—	fast	—	no	sw_pad_ctl_ld3[2]	high	—	100k pull-up	sw_pad_ctl_ld3[7]	pull	—	PP	—	no
LD4	input	pulled up	NVCC7	regular	—	fast	—	no	sw_pad_ctl_ld4[2]	high	—	100k pull-up	sw_pad_ctl_ld4[7]	pull	—	PP	—	no
LD5	input	pulled up	NVCC7	regular	—	fast	—	no	sw_pad_ctl_ld5[2]	high	—	100k pull-up	sw_pad_ctl_ld5[7]	pull	—	PP	—	no
LD6	input	pulled up	NVCC7	regular	—	fast	—	no	sw_pad_ctl_ld6[2]	high	—	100k pull-up	sw_pad_ctl_ld6[7]	pull	—	PP	—	no
LD7	input	pulled up	NVCC7	regular	—	fast	—	no	sw_pad_ctl_ld7[2]	high	—	100k pull-up	sw_pad_ctl_ld7[7]	pull	—	PP	—	no
LD8	input	pulled up	NVCC7	regular	—	fast	—	no	sw_pad_ctl_ld8[2]	high	—	100k pull-up	sw_pad_ctl_ld8[7]	pull	—	PP	—	no

Table 4-12. and i.MX31L I/O Settings (continued)

Package Contact Name	Value After Reset		Supply	I/O Type	Slew Rate		Loop back?		Drive Strength		Pull Value and Direction		Pull/Keeper Control		Open-Drain/ Push-Pull		Schmitt Trigger?	
	Direction	State			Control Bit	Default	Control Bit	Default	Control Bits	Default	Control Bits	Default	Control Bit	Default	Control Bit	Default	Control Bit	Default
LD9	input	pulled up	NVCC7	regular	—	fast	—	no	sw_pad_ctl_ld9[2]	high	—	100k pull-up	sw_pad_ctl_ld9[7]	pull	—	PP	—	no
LD10	input	pulled up	NVCC7	regular	—	fast	—	no	sw_pad_ctl_ld10[2]	high	—	100k pull-up	sw_pad_ctl_ld10[7]	pull	—	PP	—	no
LD11	input	pulled up	NVCC7	regular	—	fast	—	no	sw_pad_ctl_ld11[2]	high	—	100k pull-up	sw_pad_ctl_ld11[7]	pull	—	PP	—	no
LD12	input	pulled up	NVCC7	regular	—	fast	—	no	sw_pad_ctl_ld12[2]	high	—	100k pull-up	sw_pad_ctl_ld12[7]	pull	—	PP	—	no
LD13	input	pulled up	NVCC7	regular	—	fast	—	no	sw_pad_ctl_ld13[2]	high	—	100k pull-up	sw_pad_ctl_ld13[7]	pull	—	PP	—	no
LD14	input	pulled up	NVCC7	regular	—	fast	—	no	sw_pad_ctl_ld14[2]	high	—	100k pull-up	sw_pad_ctl_ld14[7]	pull	—	PP	—	no
LD15	input	pulled up	NVCC7	regular	—	fast	—	no	sw_pad_ctl_ld15[2]	high	—	100k pull-up	sw_pad_ctl_ld15[7]	pull	—	PP	—	no
LD16	input	pulled up	NVCC7	regular	—	fast	—	no	sw_pad_ctl_ld16[2]	high	—	100k pull-up	sw_pad_ctl_ld16[7]	pull	—	PP	—	no
LD17	input	pulled up	NVCC7	regular	—	fast	—	no	sw_pad_ctl_ld17[2]	high	—	100k pull-up	sw_pad_ctl_ld17[7]	pull	—	PP	—	no
VSYNC0	input	pulled up	NVCC7	regular	—	fast	—	no	sw_pad_ctl_vsync0[2]	high	—	100k pull-up	sw_pad_ctl_vsync0[7]	pull	—	PP	—	no
HSYNC	input	floating	NVCC7	regular	—	fast	—	no	sw_pad_ctl_hsync[2]	high	—	100k pull-up	—	disable	—	PP	—	no

Table 4-12. and i.MX31L I/O Settings (continued)

Package Contact Name	Value After Reset		Supply	I/O Type	Slew Rate		Loop back?		Drive Strength		Pull Value and Direction		Pull/Keeper Control		Open-Drain/ Push-Pull		Schmitt Trigger?	
	Direction	State			Control Bit	Default	Control Bit	Default	Control Bits	Default	Control Bits	Default	Control Bit	Default	Control Bit	Default	Control Bit	Default
FPSHIFT	input	floating	NVCC7	regular	—	fast	—	no	sw_pad_ctl_fpshift[2]	high	—	100k pull-up	—	disable	—	PP	—	no
DRDY0	input	floating	NVCC7	regular	—	fast	—	no	sw_pad_ctl_drdy0[2]	high	—	100k pull-up	—	disable	—	PP	—	no
SD_D_I	input	floating	NVCC7	regular	—	fast	—	no	sw_pad_ctl_sd_d_o[2]	high	—	100k pull-up	—	disable	—	PP	—	no
SD_D_IO	input	floating	NVCC7	regular	—	fast	—	no	sw_pad_ctl_sd_d_io[2]	high	—	100k pull-up	—	disable	—	PP	—	no
SD_D_CLK	input	floating	NVCC7	regular	—	fast	—	no	sw_pad_ctl_sd_d_clk[2]	high	—	100k pull-up	—	disable	—	PP	—	no
LCS0	input	floating	NVCC7	regular	—	fast	—	no	sw_pad_ctl_lcs0[2]	high	—	100k pull-up	—	disable	—	PP	—	no
LCS1	input	floating	NVCC7	regular	—	fast	—	no	sw_pad_ctl_lcs1[2]	high	—	100k pull-up	—	disable	—	PP	—	no
SER_RS	input	floating	NVCC7	regular	—	fast	—	no	sw_pad_ctl_ser_rs[2]	high	—	100k pull-up	—	disable	—	PP	—	no
PAR_RS	input	floating	NVCC7	regular	—	fast	—	no	sw_pad_ctl_par_rs[2]	high	—	100k pull-up	—	disable	—	PP	—	no
WRITE	input	floating	NVCC7	regular	—	fast	—	no	sw_pad_ctl_write[2]	high	—	100k pull-up	—	disable	—	PP	—	no

Table 4-12. and i.MX31L I/O Settings (continued)

Package Contact Name	Value After Reset		Supply	I/O Type	Slew Rate		Loop back?		Drive Strength		Pull Value and Direction		Pull/Keeper Control		Open-Drain/ Push-Pull		Schmitt Trigger?	
	Direction	State			Control Bit	Default	Control Bit	Default	Control Bits	Default	Control Bits	Default	Control Bit	Default	Control Bit	Default	Control Bit	Default
READ	input	floating	NVCC7	regular	—	fast	—	no	sw_pad_ctl_read[2]	high	—	100k pull-up	—	disable	—	PP	—	no
VSYNC3	input	pulled up	NVCC7	regular	—	fast	—	no	sw_pad_ctl_vsync3[2]	high	—	100k pull-up	sw_pad_ctl_vsync3[7]	pull	—	PP	—	no
CONTRAST	input	floating	NVCC7	regular	—	fast	—	no	sw_pad_ctl_contrast[2]	high	—	100k pull-up	—	disable	—	PP	—	no
D3_REV	input	floating	NVCC7	regular	—	fast	—	no	sw_pad_ctl_d3_rev[2]	high	—	100k pull-up	—	disable	—	PP	—	no
D3_CLS	input	floating	NVCC7	regular	—	fast	—	no	sw_pad_ctl_d3_cls[2]	high	—	100k pull-up	—	disable	—	PP	—	no
D3_SPL	input	floating	NVCC7	regular	—	fast	—	no	sw_pad_ctl_d3_spl[2]	high	—	100k pull-up	—	disable	—	PP	—	no
SD1_CMD	input	floating	NVCC3	regular	sw_pad_ctl_sd1_cmd[0]	fast	sw_pad_ctl_sd1_cmd[9]	no	sw_pad_ctl_sd1_cmd[2:1]	std	—	100k pull-up	—	disable	—	PP	sw_pad_ctl_sd1_cmd[4]	no
SD1_CLK	input	floating	NVCC3	regular	sw_pad_ctl_sd1_clk[0]	fast	—	no	sw_pad_ctl_sd1_clk[2:1]	std	—	100k pull-up	—	disable	—	PP	—	no
SD1_DATA0 **note 9, 10**	input	floating	NVCC3	regular	sw_pad_ctl_sd1_data0[0]	fast	sw_pad_ctl_sd1_data0[9]	no	sw_pad_ctl_sd1_data0[2:1]	std	sw_pad_ctl_sd1_data2[8]	100k pull-up	sw_pad_ctl_sd1_data0[8]	disable	—	PP	—	no

Table 4-12. and i.MX31L I/O Settings (continued)

Package Contact Name	Value After Reset		Supply	I/O Type	Slew Rate		Loop back?		Drive Strength		Pull Value and Direction		Pull/Keeper Control		Open-Drain/ Push-Pull		Schmitt Trigger?	
	Direction	State			Control Bit	Default	Control Bit	Default	Control Bits	Default	Control Bits	Default	Control Bit	Default	Control Bit	Default	Control Bit	Default
SD1_DATA1 **note 9**	input	floating	NVCC3	regular	sw_pad_ctl_sd1_data1[0]	fast	sw_pad_ctl_sd1_data1[9]	no	sw_pad_ctl_sd1_data1[2:1]	std	sw_pad_ctl_sd1_data2[8]	100k pull-up	sw_pad_ctl_sd1_data1[8]	disable	—	PP	—	no
SD1_DATA2 **note 9, 10**	input	floating	NVCC3	regular	sw_pad_ctl_sd1_data2[0]	fast	sw_pad_ctl_sd1_data2[9]	no	sw_pad_ctl_sd1_data2[2:1]	std	sw_pad_ctl_sd1_data2[8]	100k pull-up	sw_pad_ctl_sd1_data0[8]	disable	—	PP	—	no
SD1_DATA3 **note 9**	input	floating	NVCC3	regular	sw_pad_ctl_sd1_data3[0]	fast	sw_pad_ctl_sd1_data3[9]	no	sw_pad_ctl_sd1_data3[2:1]	std	sw_pad_ctl_sd1_data2[8]	100k pull-dn	sw_pad_ctl_sd1_data3[8]	disable	—	PP	—	no
Note 9: SD1_DATA[3:0] are controlled by the same Pull Value and Direction bit. 0=100k pull-down, 1=100k pull-up. **Note 10:** SD1_DATA2 and SD1_DATA0 are controlled by the same Pull/Keeper control bit.																		
ATA_CS0	input	floating	NVCC3	regular	sw_pad_ctl_ata_cs0[0]	slow	—	no	sw_pad_ctl_ata_cs0[2:1]	std		100k pull-up	—	disable	—	PP	—	no
ATA_CS1	input	floating	NVCC3	regular	sw_pad_ctl_ata_cs1[0]	slow	—	no	sw_pad_ctl_ata_cs1[2:1]	std	—	100k pull-up	—	disable	—	PP	—	no
ATA_DIOR	input	pulled up	NVCC3	regular	sw_pad_ctl_ata_dior[0]	slow	—	no	sw_pad_ctl_ata_dior[2:1]	std	—	100k pull-up	sw_pad_ctl_ata_dior[8]	pull	—	PP	—	no
ATA_DIOW	input	pulled up	NVCC3	regular	sw_pad_ctl_ata_diow[0]	slow	—	no	sw_pad_ctl_ata_diow[2:1]	std	—	100k pull-up	sw_pad_ctl_ata_diow[8]	pull	—	PP	—	no
ATA_DMACK	input	pulled up	NVCC3	regular	sw_pad_ctl_ata_dmack[0]	slow	—	no	sw_pad_ctl_ata_dmack[2:1]	std	—	100k pull-up	sw_pad_ctl_ata_dmack[8]	pull	—	PP	—	no

Table 4-12. and i.MX31L I/O Settings (continued)

Package Contact Name	Value After Reset		Supply	I/O Type	Slew Rate		Loop back?		Drive Strength		Pull Value and Direction		Pull/Keeper Control		Open-Drain/ Push-Pull		Schmitt Trigger?	
	Direction	State			Control Bit	Default	Control Bit	Default	Control Bits	Default	Control Bits	Default	Control Bit	Default	Control Bit	Default	Control Bit	Default
ATA_RESET	input	pulled up	NVCC3	regular	sw_pad_ctl_ata_reset[0]	slow	—	no	sw_pad_ctl_ata_reset[2:1]	std	—	100k pull-up	sw_pad_ctl_ata_reset[8]	pull	—	PP	—	no
CE_CONTROL **note 11**	input	floating	NVCC8	regular	—	fast	—	no	—	std	—	100k pull-dn	—	disable	—	PP	—	no
Note 11: CE_CONTROL is a reserved input and must be externally tied to GND through a 1 kΩ resistor.																		
CLKSS	input	floating	NVCC1	regular	—	fast	—	no	—	std	—	100k pull-up	—	disable	—	PP	—	no
CSPI3_MOSI	input	pulled up	NVCC3	regular	sw_pad_ctl_cspi3_mosi[0]	slow	—	no	sw_pad_ctl_cspi3_mosi[2:1]	std	—	100k pull-up	sw_pad_ctl_cspi3_mosi[8]	pull	—	PP	—	no
CSPI3_MISO	input	pulled up	NVCC3	regular	sw_pad_ctl_cspi3_miso[0]	slow	—	no	sw_pad_ctl_cspi3_miso[2:1]	std	—	100k pull-up	sw_pad_ctl_cspi3_miso[8]	pull	—	PP	—	no
CSPI3_SCLK	input	pulled up	NVCC3	regular	sw_pad_ctl_cspi3_sclk[0]	slow	—	no	sw_pad_ctl_cspi3_sclk[2:1]	std	—	100k pull-up	sw_pad_ctl_cspi3_sclk[8]	pull	—	PP	sw_pad_ctl_cspi3_sclk[4]	yes
CSPI3_SPI_RDY	input	pulled up	NVCC3	regular	sw_pad_ctl_cspi3_spi_rdy[0]	slow	—	no	sw_pad_ctl_cspi3_spi_rdy[2:1]	std	—	100k pull-up	sw_pad_ctl_cspi3_spi_rdy[8]	pull	—	PP	—	no
TTM_PAD	—	pulled down	NVCC7	regular	—	slow	—	no	—	std	—	100k pull-dn [1]	—	disable[1]	—	PP	—	no

[1] TTM_PAD is for Freescale factory use only. Control bits indicate pull-up/down disabled. However, TTM_PAD is actually connected to an on-chip pull-down device. Users must float this signal or tie it to GND.

4.4.4 EMI Signal Multiplexing

The EMI signal multiplexing described in this section deals with multiplexing that is performed in the EMI. This type of multiplexing is performed automatically whenever the processor accesses a particular memory space that is controlled by one of the four memory controllers: EIM, ESDCTL (SDRAM-SDR or SDRAM-DDR), PCMCIA, or NFC. See Table 4-13 for details.

Table 4-13. EMI Signal Multiplexing

Contact Name	I/O Type	EIM	SDRAM SDR	PCMCIA	SDRAM DDR	NFC
A0	regular	A0	MA0	A0	MA0	—
A1	regular	A1	MA1	A1	MA1	—
A2	regular	A2	MA2	A2	MA2	—
A3	regular	A3	MA3	A3	MA3	—
A4	regular	A4	MA4	A4	MA4	—
A5	regular	A5	MA5	A5	MA5	—
A6	regular	A6	MA6	A6	MA6	—
A7	regular	A7	MA7	A7	MA7	—
A8	regular	A8	MA8	A8	MA8	—
A9	regular	A9	MA9	A9	MA9	—
A10	regular	A10	—	A10	—	—
MA10	regular	—	MA10	—	MA10	—
A11	regular	A11	MA11	A11	MA11	—
A12	regular	A12	MA12	A12	MA12	—
A13	regular	A13	MA13	A13	MA13	—
A14	regular	A14	—	A14	—	—
A15	regular	A15	—	A15	—	—
A16	regular	A16	—	A16	—	—
A17	regular	A17	—	A17	—	—
A18	regular	A18	—	A18	—	—
A19	regular	A19	—	A19	—	—
A20	regular	A20	—	A20	—	—
A21	regular	A21	—	A21	—	—
A22	regular	A22	—	A22	—	—
A23	regular	A23	—	A23	—	—
A24	regular	A24	—	A24	—	—
A25	regular	A25	—	A25	—	—

Table 4-13. EMI Signal Multiplexing (continued)

Contact Name	I/O Type	EIM	SDRAM SDR	PCMCIA	SDRAM DDR	NFC
SDBA1	regular	—	SDBA1	$\overline{CE1}$	SDBA1	—
SDBA0	regular	—	SDBA0	$\overline{CE2}$	SDBA0	—
SD0	ddr	—	SD0	—	SD0	—
SD1	ddr	—	SD1	—	SD1	—
SD2	ddr	—	SD2	—	SD2	—
SD3	ddr	—	SD3	—	SD3	—
SD4	ddr	—	SD4	—	SD4	—
SD5	ddr	—	SD5	—	SD5	—
SD6	ddr	—	SD6	—	SD6	—
SD7	ddr	—	SD7	—	SD7	—
SD8	ddr	—	SD8	—	SD8	—
SD9	ddr	—	SD9	—	SD9	—
SD10	ddr	—	SD10	—	SD10	—
SD11	ddr	—	SD11	—	SD11	—
SD12	ddr	—	SD12	—	SD12	—
SD13	ddr	—	SD13	—	SD13	—
SD14	ddr	—	SD14	—	SD14	—
SD15	ddr	—	SD15	—	SD15	—
SD16	ddr	—	SD16	—	SD16	—
SD17	ddr	—	SD17	—	SD17	—
SD18	ddr	—	SD18	—	SD18	—
SD19	ddr	—	SD19	—	SD19	—
SD20	ddr	—	SD20	—	SD20	—
SD21	ddr	—	SD21	—	SD21	—
SD22	ddr	—	SD22	—	SD22	—
SD23	ddr	—	SD23	—	SD23	—
SD24	ddr	—	SD24	—	SD24	—
SD25	ddr	—	SD25	—	SD25	—
SD26	ddr	—	SD26	—	SD26	—
SD27	ddr	—	SD27	—	SD27	—
SD28	ddr	—	SD28	—	SD28	—
SD29	ddr	—	SD29	—	SD29	—

Table 4-13. EMI Signal Multiplexing (continued)

Contact Name	I/O Type	EIM	SDRAM SDR	PCMCIA	SDRAM DDR	NFC
SD30	ddr	—	SD30	—	SD30	—
SD31	ddr	—	SD31	—	SD31	—
DQM0	ddr	—	DQM0	—	DQM0	—
DQM1	ddr	—	DQM1	—	DQM1	—
DQM2	ddr	—	DQM2	—	DQM2	—
DQM3	ddr	—	DQM3	—	DQM3	—
EB0	regular	EB0	—	REG	—	—
EB1	regular	EB1	—	IORD	—	—
OE	regular	OE	—	IOWR	—	—
CS0	regular	CS0	—	—	—	—
CS1	regular	CS1	—	—	—	—
CS2	regular	CS2	CSD0	—	CSD0	—
CS3	regular	CS3	CSD1	—	CSD1	—
CS4	regular	CS4	—	—	—	—
CS5	regular	CS5	—	—	—	—
ECB	regular	ECB	—	—	—	—
LBA	regular	LBA	—	$\overline{OE}$	—	—
BCLK	regular	BCLK	—	—	—	—
RW	regular	RW	—	WE	—	—
RAS	regular	—	RAS	—	RAS	—
CAS	regular	—	CAS	—	CAS	—
SDWE	regular	—	SDWE	—	SDWE	—
SDCKE0	regular	—	SDCKE0	—	SDCKE0	—
SDCKE1	regular	—	SDCKE1	—	SDCKE1	—
SDCLK	regular	—	SDCLK	—	SDCLK	—
$\overline{SDCLK}$	regular	—	—	—	$\overline{SDCLK}$	—
SDQS0	ddr	—	—	—	SDQS0	—
SDQS1	ddr	—	—	—	SDQS1	—
SDQS2	ddr	—	—	—	SDQS2	—
SDQS3	ddr	—	—	—	SDQS3	—
$\overline{NFWE}$	regular	—	—	—	—	WE
$\overline{NFRE}$	regular	—	—	—	—	RE

Table 4-13. EMI Signal Multiplexing (continued)

Contact Name	I/O Type	EIM	SDRAM SDR	PCMCIA	SDRAM DDR	NFC
NFALE	regular	—	—	—	—	ALE
NFCLE	regular	—	—	—	—	CLE
$\overline{\text{NFWP}}$	regular	—	—	—	—	WP
$\overline{\text{NFCE}}$	regular	—	—	—	—	CE
NFRB	regular	—	—	—	—	R/B
D15	regular	D15	—	D15	—	D15
D14	regular	D14	—	D14	—	D14
D13	regular	D13	—	D13	—	D13
D12	regular	D12	—	D12	—	D12
D11	regular	D11	—	D11	—	D11
D10	regular	D10	—	D10	—	D10
D9	regular	D9	—	D9	—	D9
D8	regular	D8	—	D8	—	D8
D7	regular	D7	—	D7	—	D7
D6	regular	D6	—	D6	—	D6
D5	regular	D5	—	D5	—	D5
D4	regular	D4	—	D4	—	D4
D3	regular	D3	—	D3	—	D3
D2	regular	D2	—	D2	—	D2
D1	regular	D1	—	D1	—	D1
D0	regular	D0	—	D0	—	D0
$\overline{\text{PC\_CD1}}$	regular	—	—	CD1_B	—	—
$\overline{\text{PC\_CD2}}$	regular	—	—	CD2_B	—	—
$\overline{\text{PC\_WAIT}}$	regular	—	—	WAIT_B	—	—
PC_READY	regular	—	—	READY	—	—
PC_PWRON	regular	—	—	PC_PWRON	—	—
PC_VS1	regular	—	—	VS1	—	—
PC_VS2	regular	—	—	VS2	—	—
PC_BVD1	regular	—	—	BVD1	—	—
PC_BVD2	regular	—	—	BVD2	—	—
PC_RST	regular	—	—	RST	—	—
IOIS16	regular	—	—	IOIS16/WP	—	—

Table 4-13. EMI Signal Multiplexing (continued)

Contact Name	I/O Type	EIM	SDRAM SDR	PCMCIA	SDRAM DDR	NFC
$\overline{\text{PC\_RW}}$	regular	—	—	RW_B	—	—
PC_POE	regular	—	—	POE	—	—

4.5 Special I/O Signal Considerations

The following I/O lines should be connected as described in the following sections.

4.5.1 Power Ready Input (GPIO1_5)

The i.MX31/31L uses the Power Ready input as a qualifier when exiting state retention mode. The power ready input, GPIO1_5, should be connected to an external power management IC power ready output signal. If not used, GPIO1_5 must either be (a) externally pulled-up to NVCC1 or (b) a no connect, internally pulled-up by enabling the on-chip pull-up resistor. GPIO1_5 is a dedicated input and cannot be used as a general-purpose input/output.

4.5.2 SJC_MOD

SJC_MOD must be externally connected to GND for normal operation. Termination to GND through an external pull-down resistor (such as 1 kΩ) is allowed, but the value should be much smaller than the on-chip 100 kΩ pull-up.

4.5.3 CE_CONTROL

CE_CONTROL is a reserved input and must be externally tied to GND through a 1 kΩ resistor.

4.5.4 TTM_PAD

TTM_PAD is for Freescale factory use only. Control bits indicate pull-up/down disabled. However, TTM_PAD is actually connected to an on-chip pull-down device. Users must either float this signal or tie it to GND.

4.5.5 M_REQUEST and M_GRANT

These two signals are not utilized internally. The user should make no connection to these signals.

4.5.6 External DMA Signals (EXTDMA)

Input signals EXTDMA_0, EXTDMA_1, and EXTDMA_2 (also called EXTDMAREQ1, EXTDMAREQ2, and EXTDMAREQ3) are used as external DMA request event signals and are designed to trigger internal DMA transactions. This type of functionality is analogous to interrupt requests. These

signals should not be used to trigger memory-to-memory DMA transactions. The SDMA script for memory-to-memory transfers is not designed to clear the SDMA request event when the DMA transaction is complete.

To trigger SDMA transfers to/from the WEIM, ESDCTL, or NAND Flash Controller, the external DMA request signals should be configured as a GPIO interrupt, where the interrupt service routine initiates the memory-to-memory DMA transfer. The i.MX31/31L do not provide external bus mastership. DMA-style transactions on the external bus (those requiring both a DMA request and DMA grant or acknowledge) are not supported. These external request signals are accessed by invoking Alternate Mode 1 on GPIO1_0, GPIO1_1, and GPIO1_2.

4.5.7 Tamper Detect Logic

Tamper detect logic is used to issue a security violation. This logic is activated if the tamper detect input is asserted.

The tamper detect logic is disabled after reset. After enabling the logic, it is impossible to disable it until the next reset. The GPR[16] bit functions as the tamper detect enable bit.

GPIO1_6 functions similarly to other I/O with GPIO capabilities regardless of the status of the tamper detect enable bit. (For example, the GPIO1_6 can function as an input with GPIO capabilities, such as sampling through PSR or generating interrupts.)

4.5.8 Clock Source Select (CLKSS)

The CLKSS is the input that selects the default reference clock source providing input to the DPLL. To select CKIH, tie CLKSS to NVCC1. To select CKIL, tie CLKSS to ground. After initialization, the reference clock source can be changed (initial setting is overwritten) by programming the PRCS bits in the CCMR.

Chapter 13
IC Identification (IIM)

The IC Identification Module (IIM) provides an interface for reading and, in some cases, programming and/or overriding identification and control information stored in on-chip fuse elements.

The IIM also provides a set of volatile software-accessible signals that can be used for software control of hardware elements, not requiring non-volatility.

13.1 Overview

The IIM provides the primary user-visible mechanism for interfacing with on-chip fuse elements. Among the uses for the fuses are unique chip identifiers, mask revision numbers, cryptographic keys, and various control signals requiring permanent non-volatility. The IIM also provides up to 28 volatile control signals and the means to generate a second 168-bit SCC key.

The IIM consists of a master controller, a software fuse value shadow cache, and a set of registers to hold the values of signals visible outside the module. Up to eight arrays of fuses (e-Fuses) are associated with the IIM.

The IIM is accessible using an 8-bit SkyBlue IP bus interface. An 8-bit interface is used because it matches the natural width of the fuse arrays. All registers are 32-bit aligned to allow the module to be instantiated on IP buses supporting only 32-bit peripherals.

13.1.1 Features

The following are the IIM features:

- Up to eight independent fuse banks (number of fuse bank and size of the bank are parameterized)
- Maximum usable fuse bank size is 2048 bits
- e-Fuse banks may be intermixed on a per bank basis
- Support for driving secure JTAG challenge and response values to the SJC (size of each field configurable using RTL parameter; challenge default size is 64 bits, response default size is 56 bits)
- Ability to provide up to two distinct 168-bit 3DES keys from a single set of fuses
- Ability to override fuse values in software (does not affect the fuse element); override capability can be permanently disabled on a per-bank basis
- Ability to write-protect e-Fuses on a per-bank basis
- Ability to scan-protect (read and program) on a per-bank basis
- Fuses may be programmed by software, directly by JTAG, or indirectly by JTAG using a processor.
- Recommended signal assignments to maximize software re-use

13.2 Memory Map and Register Definition

Section 13.2.2.1, "Silicon Revision (SREV)" provides the detailed register description for the SREV register.

13.2.1 Memory Map

The IIM register is eight bits wide, but addressable on 32-bit boundaries. Only the bottom eight bits (the usable bits) of the register is shown in Figure 13-2. The top 24 bits is always read as 0 and writes to them are ignored.

13.2.2 Register Summary

Figure 13-1 shows the key to the register fields

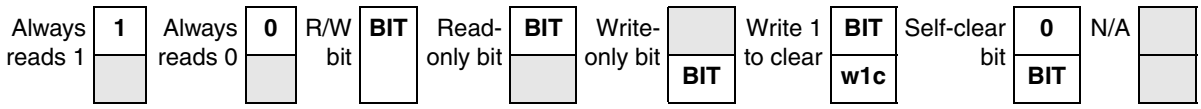

Figure 13-1. Key to Register Fields

13.2.2.1 Silicon Revision (SREV)

SREV is the silicon revision (that is, mask revision) register, which corresponds to the bottom eight bits of the deprecated HW_REV register. See Figure 13-2 for an illustration of valid bits in the Silicon Revision Register, Table 13-1 for its field descriptions, and Table 13-2 for the SILICON_REV settings.

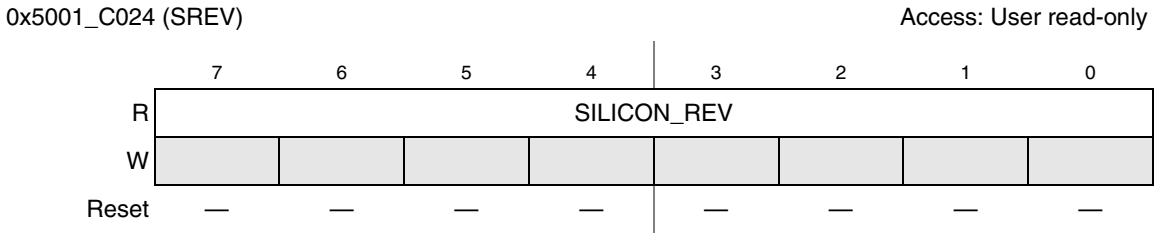

Figure 13-2. Silicon Revision Register

Table 13-1. Silicon Revision Register Field Descriptions

Field	Description
7–0 SILICON_REV	Mask Set Revision. The mask set revision used in the fabrication of the part. The value changes with each change to the mask set. See Table 13-2 for the revision settings.

Table 13-2. SILICON_REV Settings

SREV	Device	Silicon Revision	Device Marking Wafer Fab 1	Device Marking Wafer Fab 2
0x00	i.MX31 and i.MX31L	1.0	L38W	—
0x10	i.MX31	1.1	2L38W	—
0x11	i.MX31L	1.1	2L38W	—
0x12	i.MX31	1.15	2L38W 3L38W[1]	—
0x13	i.MX31L	1.15	2L38W 3L38W[1]	—
0x14	i.MX31	1.2	3L38W[2]	M45G
0x15	i.MX31L	1.2	3L38W[3]	M45G

1 Mismarked device. IC stamped 3L38W, SREV register reads correct value: 2L38W. The device marking has the initial characters MCIMX31.

2 Non-production part used for population of ADS boards. The device marking has the initial characters PCIMX31.

3 This is a non-production part and is not available. The device marking has the initial characters PCIMX31.

NOTE

Contact your Freescale Semiconductor sales office or distributor for additional information.

Chapter 19
Enhanced SDRAM Controller (ESDCTL)

19.4.6 SDRAM (SDR and LPDDR) Command Encoding

Table 19-32 summarizes the command encoding utilized by this controller. These commands represent a subset of the commands defined by the JEDEC standard.

Table 19-32. SDRAM (SDR and LPDDR) Command Encoding

Function	Symbol	CKE n-1	CKE n	CS	RAS	CAS	WE	A11	A10	BA[1:0]	A[13:0]
Deselect	DSEL	H	X	H	X	X	X	X	X	X	X
No Operation	NOP	H	X	L	H	H	H	X	X	X	X
Read	READ	H	X	L	H	L	H	V	L	V	V
Write	WRIT	H	X	L	H	L	L	V	L	V	V
Bank Activate	ACT	H	X	L	L	H	H	V	V	V	V
Burst Terminate[1]	TBST	H	X	L	H	H	L	X	X	V	X
Precharge Select Bank	PRE	H	X	L	L	H	L	V	L	V	X
Precharge All Banks	PALL	H	X	L	L	H	L	X	H	X	X
Auto-Refresh	CBR	H	X	L	L	L	H	X	X	X	X
Self Refresh Entry	SLFRSH	H	L	L	L	L	H	X	X	X	X
Self Refresh Exit	SLFRSHX	L	H	H	X	X	X	X	X	X	X
Power-Down Entry	PWRDN	H	L	H	X	X	X	X	X	X	X
Power-Down Exit	PWRDNX	L	H	H	X	X	X	X	X	X	X
Mode Register Set[2]	MRS	H	X	L	L	L	L	L	L	V	V

[1]For Mobile DDR, applies only to read bursts (with auto precharge disabled).
[2]BA0-BA1 select either the mode register, the extended mode register or the LOW POWER extended mode register.