Armadillo-210

Hardware Manual

Version 1.0.1 Pre1

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Atmark Techno, Inc.
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1. Introduction

Thank you for your purchase of the Armadillo-210.

The Armadillo-210 is an ARM9 processor (CirrusLogic's EP9307) based microcomputer equipped with 10BASE-T/100BASE-TX (Power over Ethernet/IEEE802.3af), RS232C serial interface and general-purpose I/O.

The Armadillo-210 uses Linux as standard operating system (OS). It allows leveraging a wide variety of software assets which have been developed using open sources. It also allows using GNU assembler and C-compiler for software development.

■

This manual introduces the Armadillo-210 hardware specifications and how to use it. We hope the information contained in this document will help you get the best functionality out of the Armadillo-210.

2. Precautions

2.1. Safety Precautions

Before using the Armadillo-210, please read the following safety precautions carefully to assure correct use.

This product uses semiconductor components designed for generic electronics equipment such as office automation equipment, communications equipment, measurement equipment and machine tools. Do not incorporate the product into devices such as medical equipment, traffic control systems, combustion control systems, safety equipment and so on which can directly threaten human life or pose a hazard to the body or property due to malfunction or failure. Moreover, products incorporating semiconductor components can be caused to malfunction or fail due to foreign noise or surge. To ensure there will be no risk to life, the body or property even in the event of malfunction or failure, be sure to take all possible measures in the safety system design, such as using protection circuits like limit switches or fuse breakers, or system multiplexing.

2.2. Operational Precautions

To avoid a permanent damage to the Armadillo-210, the following safety precautions must be observed when handling the product.

- **Power-on**
  Do not attempt to install or remove the GPIO connectors when power is applied to the Armadillo-210 or peripheral circuits.

- **Static-Electricity**
  The Armadillo-210 incorporates CMOS devices. Until using the board, store it in the provided antistatic package

- **Latch-up**
  Due to excessive noise or a surge from the power supply or input/output, or sharp voltage fluctuations, the CMOS devices incorporated in the board can cause a latch-up. Once a latch-up occurs, this situation continues until the power supply is disconnected and thus can damage the devices. It is recommended to take safety measures such as adding a protection circuit to the noise-susceptible input/output line or not sharing a power supply with devices that can be the cause of noise.

2.3. Software Precautions

- The software and documentation contained in this product are provided “AS IS” without warranty of any kind including any warranty of merchantability or fitness for a particular purposes, reliability, correctness or accuracy. Furthermore, Atmark Techno, Inc. does not guarantee any outcomes resulting from the use of this product

2.4. Trademarks

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3. Overview

3.1. Board Overview

The Armadillo-210 main specifications are shown in Table 3-1.

Table 3-1 Armadillo-210 Board Specifications

Processor	CirrusLogic EP9307 ARM920T core ・ARM9TDMI CPU ・16kByte instruction cache ・16kByte data cache ・Thumb code (16bit instruction set) supported
System Clock	CPU Core clock: 200MHz BUS clock: 100MHz
Memory	SDRAM: 32MByte (16bit width) FLASH: 4MByte (16bit width)
LAN Interface	10BASE-T/100BASE-TX Power over Ethernet (compliant with IEEE802.3af) * Compatible with devices feeding with LAN connector's 4/5-pin pair and 7/8-pin pair
Serial Port	2 channels (asynchronous, Max: 230.4kbps) COM1: ・RS232C level input/output ・Flow control pins (CTS,RTS,DTR,DSR,DCD and RI) COM2: ・3.3V I/O level input/output ・No flow control pins
General Purpose Parallel Input/Output	8bits
Timer	・16bit general-purpose timer: 2 channels (one channel is used for Linux system timer) ・32bit general-purpose timer: 1 channel ・40bit debug timer: 1 channel
Board Dimension (mm)	37.5 × 50.0 (exclusive of protrusions)
Case Dimension (mm)	45.0 × 79.0 × 26.5 (exclusive of protrusions)
Power Voltage	DC9V - 48V
Power Consumption	1.2W (Typ.)

3.2. Block Diagram

Armadillo-210 block diagram is shown in Figure 3-1.

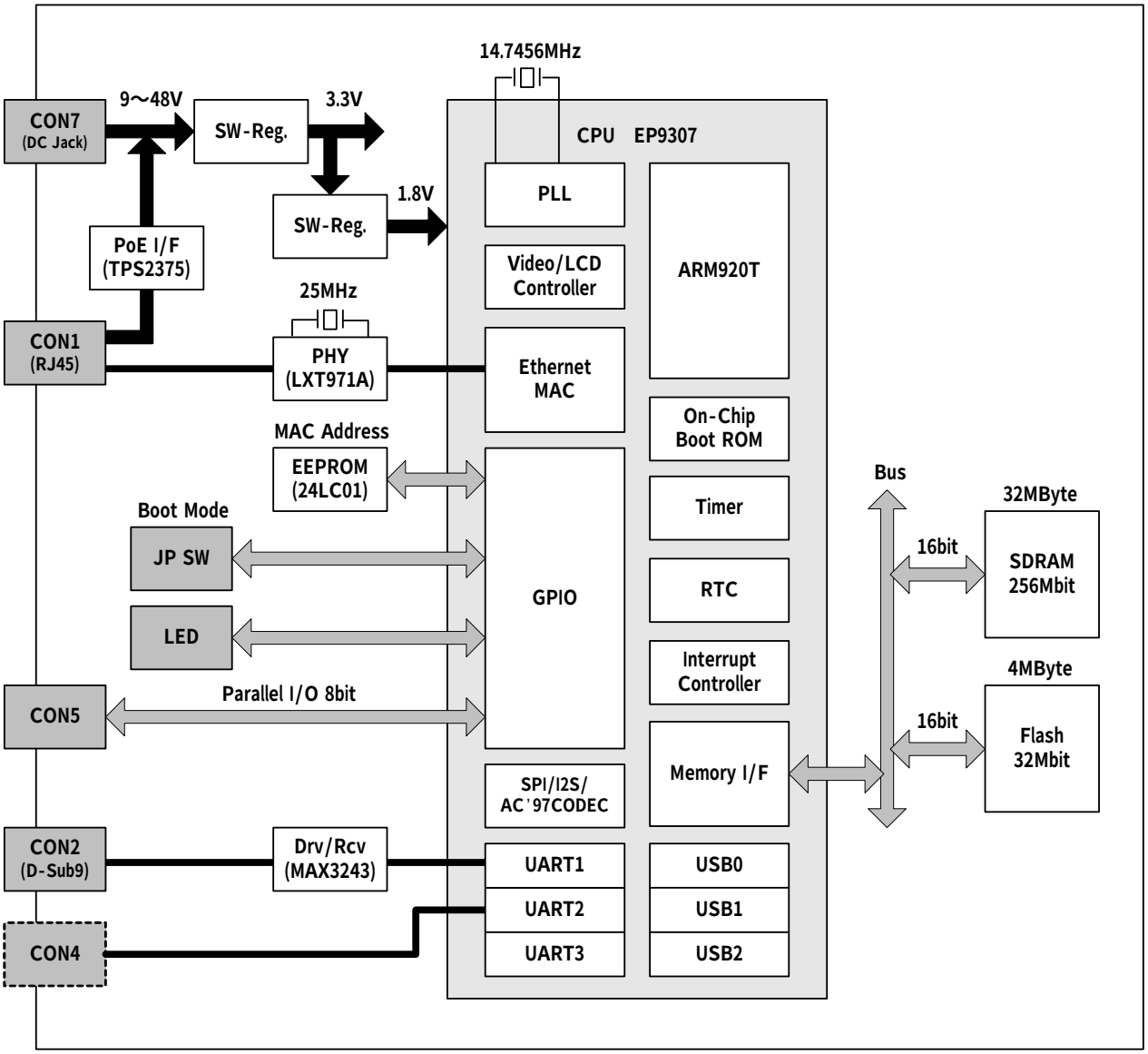


Figure 3-1 Armadillo-210 Block Diagram

4. Memory Map

4.1. Physical Memory Map

Armadillo-210 physical memory map is shown in Table 4-1.

Table 4-1 Armadillo-210 Memory Map

Start Address	End Address	Device	Memory Area	Set Value
0x0000 0000	0x0FFF FFFF	Reserved	CS0	
0x1000 0000	0x1FFF FFFF	Reserved	CS1	
0x2000 0000	0x2FFF FFFF	Reserved	CS2	
0x3000 0000	0x3FFF FFFF	Reserved	CS3	
0x4000 0000	0x4FFF FFFF	Reserved		
0x5000 0000	0x5FFF FFFF	Reserved		
0x6000 0000	0x603F FFFF	Flash Memory (4MByte)	CS6	16bit width
0x6040 0000	0x6FFF FFFF	Reserved		
0x7000 0000	0x7FFF FFFF	Reserved	CS7	
0x8000 0000	0x8008 FFFF	EP9307 Internal Register (AHB)	CPU System Register	
0x8009 0000	0x8009 3FFF	Internal Boot ROM (16KByte)		
0x8009 4000	0x800A FFFF	Reserved		
0x800B 0000	0x800F FFFF	EP9307 Internal Register (AHB)		
0x8010 0000	0x807F FFFF	Reserved		
0x8080 0000	0x8094 FFFF	EP9307 Internal Register (APB)		
0x8095 0000	0x8FFF FFFF	Reserved		
0x9000 0000	0xBFFF FFFF	Reserved		
0xC000 0000	0xC07F FFFF	SDRAM (8MByte)	SDCE0	16bit width
0xC080 0000	0xC0FF FFFF	Reserved		
0xC100 0000	0xC17F FFFF	SDRAM (8MByte)		
0xC180 0000	0xC3FF FFFF	Reserved		
0xC400 0000	0xC47F FFFF	SDRAM (8MByte)		
0xC480 0000	0xC4FF FFFF	Reserved		
0xC500 0000	0xC57F FFFF	SDRAM (8MByte)		
0xC580 0000	0xCFFF FFFF	Reserved		
0xD000 0000	0xDFFF FFFF	Reserved	SDCE1	
0xE000 0000	0xEFFF FFFF	Reserved	SDCE2	
0xF000 0000	0xFFFF FFFF	Reserved	SDCE3	

4.2. Logical Memory Map When Using Linux

When using Linux, the Armadillo-210 is mapped to the following logical memory map via MMU.

Table 4-2 Logical Memory Map When Using Linux

Start Address	End Address	Device	Memory Area	Set Value
Dynamic	+0x003F FFFF	Flash Memory (4MByte)	CS6	16bit width
0xC000 0000	0xC1FF FFFF	SDRAM (32MByte)	SDCE0	16bit width
0xC200 0000	0xCFFF FFFF	Reserved		
0xD000 0000	0xFEFF FFFF	Reserved		
0xFF00 0000	0xFF08 FFFF	EP9307 Internal Register (AHB)	CPU System Register	
0xFF09 0000	0xFF09 3FFF	Internal Boot ROM (16KByte)		
0xFF09 4000	0xFF0A FFFF	Reserved		
0xFF0B 0000	0xFF0F FFFF	EP9307 Internal Register (AHB)		
0xFF10 0000	0xFF7F FFFF	Reserved		
0xFF80 0000	0xFF94 FFFF	EP9307 Internal Register (APB)		
0xFF95 0000	0xFFFF FFFF	Reserved		

5. Interface Specifications

5.1. Layout of Interfaces

The layout of the Armadillo-210 interfaces is shown in Figure 5-1.

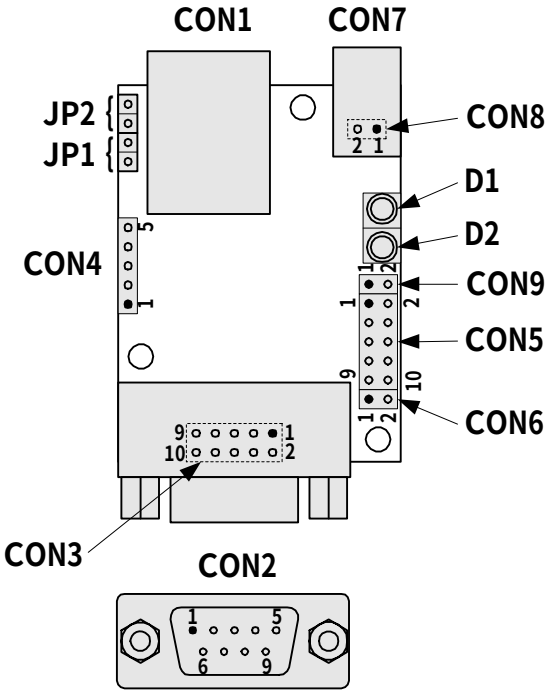


Figure 5-1 Layout of Interfaces

Table 5-1 Details of Interfaces

Symbol	Interface	Shape	Remarks
CON1	LAN Connector (10BASE-T/100BASE-TX)	RJ-45	
CON2	Serial Interface 1	D-Sub9 pin (male)	
CON3	Serial Interface 1	10-pin (2.54mm pitch)	Connector not mounted
CON4	Serial Interface 2	5-pin (2.54mm pitch)	Connector not mounted
CON5	Parallel Interface (8bit GPIO)	10-pin (2.54mm pitch)	Connector not mounted
CON6	External Reset/GPIO terminal	2-pin (2.54mm pitch)	Connector not mounted
CON7	Power Input Connector	DC Jack	
CON8	Power Input Terminal	2-pin (2.54mm pitch)	Connector not mounted
CON9	Power Output Terminal	2-pin (2.54mm pitch)	Connector not mounted
D1	Status LED (Green)	LED	
D2	Status LED (Red)	LED	
JP1	Jumper for Setting Boot Mode	2-pin (2.54mm pitch)	
JP2	Jumper for Setting Boot Mode	2-pin (2.54mm pitch)	

5.2. CON1 (LAN Connector)

CON1 is a 10BASE-T/100BASE-TX LAN interface. It can be connected to an Ethernet cable of category 5 or higher. Normally, it is connected to the hub via a straight cable. Using a cross-cable, you can connect it directly to your PC.
It also supports Power over Ethernet (IEEE802.3af) thus allowing the supply of power over Ethernet cable using a PoE power feeder that is capable of supplying power using LAN connector's (4),(5) pin pair and (7),(8) pin pair.

Note 1: When using Power over Ethernet, use a cable with all wires installed.

Note 2: When a LAN connector is reconnected while Power over Ethernet is used, supply of power may be delayed for a few seconds at the HUB side due to the operational confirmation of a power receiving device. This is not an operational problem.

Table 5-2 LAN Signal Assignment

Pin#	Signal Name	I/O	Function
1	TX＋	Out	Differential twisted pair transmit output (+)
2	TX－	Out	Differential twisted pair transmit output (-)
3	RX＋	In	Differential twisted pair receive input (+)
4	VETH＋	-	Power over Ethernet (IEEE802.3af) power supply +
5	VETH＋	-	Power over Ethernet (IEEE802.3af) power supply +
6	RX－	In	Differential twisted pair receive input (-)
7	VETH－	-	Power over Ethernet (IEEE802.3af) power supply -
8	VETH－	-	Power over Ethernet (IEEE802.3af) power supply -

5.3. CON2/CON3 (Serial Interface 1)

CON2 and CON3 is an asynchronous serial interface. It is connected to UART1, CPU (EP9307). CON2 and CON3 differ in shape and pin assignment, but they have common serial signals.

- Signal input/output level: RS232C level
- Maximum data transfer rate: 230.4kbps
- Flow control: CTS, RTS, DTR, DSR, DCD, RI
- FIFO: 16Byte built-in for both in and out
- CON2: D-Sub9 pin connector
- CON3: 10 pin connector (2×5, 2.54mm pitch)

Table 5-3 CON2 Signal Assignment

Pin#	Signal Name	I/O	Function
1	DCD1	In	Connecting to EP9307's EGPIO1(Port A:1) pin
2	RXD1	In	Connecting to EP9307's built-in UART1-RXD pin
3	TXD1	Out	Connecting to EP9307's built-in UART1-TXD pin
4	DTR1	Out	Connecting to EP9307's built-in UART1-DTR pin
5	GND	Power	Power supply (GND)
6	DSR1	In	Connecting to EP9307's built-in UART1-DSR pin
7	RTS1	Out	Connecting to EP9307's built-in UART1-RTS pin
8	CTS1	In	Connecting to EP9307's built-in UART1-CTS pin
9	RI1	In	Connecting to EP9307's EGPIO0 (Port A:0) pin

Table 5-4 CON3 Signal Assignment

Pin#	Signal Name	I/O	Function
1	DCD1	In	Connecting to EP9307's EGPIO1(Port A:1) pin
2	DSR1	In	Connecting to EP9307's built-in UART1-DSR pin
3	RXD1	In	Connecting to EP9307's built-in UART1-RXD pin
4	RTS1	Out	Connecting to EP9307's built-in UART1-RTS pin
5	TXD1	Out	Connecting to EP9307's built-in UART1-TXD pin
6	CTS1	In	Connecting to EP9307's built-in UART1-CTS pin
7	DTR1	Out	Connecting to EP9307's built-in UART1-DTR pin
8	RI1	In	Connecting to EP9307's EGPIO0(Port A:0) pin
9	GND	Power	Power supply (GND)
10	+3.3V	Power	Power supply (+3.3V) * Output current in total of CON3/CON4/CON5: 100mA Max.

5.4. CON4 (Serial Interface 2)

CON4 is an asynchronous serial interface. It is connected to UART2, CPU (EP9307).

- Signal input/output level: 3.3V I/O level
- Maximum data transfer rate: 230.4kbps
- Flow control: None
- FIFO: 16Byte built-in for both in and out

Table 5-5 CON4 Signal Assignment

Pin#	Signal Name	I/O	Function
1	GPIO	In/Out	Connecting to EP9307's EGPIO2 (Port A:2) pin
2	RXD2	In	Connecting to EP9307's built-in UART2-RXD pin
3	TXD2	Out	Connecting to EP9307's built-in UART2-TXD pin
4	+3.3V	Power	Power supply (+3.3V) * Output current in total of CON3/CON4/CON5: 100mA Max.
5	GND	Power	Power supply (GND)

5.5. CON5 (Parallel Interface)

CON5 is a general purpose input/output port. It is connected to CPU (EP9307)'s GPIO (General Purpose I/O). It can be controlled using PADR (Port A data register I/O: 0x8084 0000), PADDR (Port A data direction register I/O: 0x8084 0010), PBDR (Port B data register I/O: 0x8084 0004) and PBDDR (Port B data direction register I/O: 0x8084 0014) within EP9307.

Caution: EP9307's PortB:4 to 7 are used by the internal circuit. Do not change this setting.

Table 5-6 CON5 Signal Assignment

Pin#	Signal Name	I/O	Function
1	GND	Power	Power supply (GND)
2	+3.3V	Power	Power supply (+3.3V) * Total output current for CON3/CON4/CON5: 100mA Max.
3	GPIO_0	In/Out	Connecting to GPIO port 0 (EP9307's EGPIO4 (Port A:4) pin
4	GPIO_1	In/Out	Connecting to GPIO port 1 (EP9307's EGPIO5 (Port A:5) pin
5	GPIO_2	In/Out	Connecting to GPIO port 2 (EP9307's EGPIO6 (Port A:6) pin
6	GPIO_3	In/Out	Connecting to GPIO port 3 (EP9307's EGPIO7 (Port A:7) pin
7	GPIO_4	In/Out	Connecting to GPIO port 4 (EP9307's EGPIO8 (Port B:0) pin
8	GPIO_5	In/Out	Connecting to GPIO port 5 (EP9307's EGPIO9 (Port B:1) pin
9	GPIO_6	In/Out	Connecting to GPIO port 6 (EP9307's EGPIO10 (Port B:2) pin
10	GPIO_7	In/Out	Connecting to GPIO port 7 (EP9307's EGPIO11 (Port B:3) pin

Electrical specifications of the parallel interface are shown in Table 5-7.

Table 5-7 Electrical Specifications of the Parallel Interface

Symbol	Parameter	Min	Max	Unit	Conditions
VIH	CMOS Input high voltage	0.65×VDDIO	VDDIO+0.3	V	VDDIO=3.3V
VIL	CMOS Input low voltage	- 0.3	0.35×VDDIO	V	
VOH	CMOS Output high voltage	2.8		V	IOH=4mA
VOL	CMOS Output low voltage		0.5	V	IOL= - 4mA
IOH	High level Output current		4	mA	
IOL	Low level Output current		- 4	mA	
IIL	Input leakage current		10.0	μA	VIN=VDD or GND

5.6. CON6 (External Reset/GPIO Terminal)

CON6 is connected to the external reset IC and the CPU (EP9307)'s GPIO (General Purpose I/O).

Table 5-8 CON6 Signal Assignment

Pin#	Signal Name	I/O	Function
1	EXT_RESET*	In	The pin is connected to reset IC. Connecting the pin to the ground will assert the reset signal to the system. * Open collector and open drain signals can also be input. * High level signals are not acceptable.
2	EXTINT	In/Out	Connecting to EP9307's GPIO (Port F:7) pin

5.7. CON7/CON8 (Power Input Connector)

CON7 is a DC jack that supplies power to the Armadillo-210 and CON8 is a 2-pin connector that supplies power to the Armadillo-210.
The input voltage range is DC9V to 48V. The AC adapter jack is 5.5mm in circumference and 2.1mm in pin hole. Those AC adapters having the same polarity mark as shown in Figure 5-2 can be used.
In addition to the power input from the DC jack or the CON8, the Armadillo-210 can support Power over Ethernet*.

Power over Ethernet (IEEE802.3af) is the standard for a system to supply electrical power to remote devices over standard LAN cable.

Note 1: *If an AC adapter with high-voltage specification exceeding 12V is used, a high-voltage spark can generate at the contact part when a plug is connected to the Armadillo-210. Therefore, be sure to first connect the Armadillo-210 to the AC adapter and then connect the AC adapter to the outlet.*

Note 2: *If power has been restored to the Armadillo-210 in a very short time interval, it may keep in reset mode and not boot up. Therefore, be sure to leave over 30 milliseconds before restoring power.*

Figure 5-2 Polarity Mark on AC Adapter

Table 5-9 CON8 Signal Assignment

Pin#	Signal Name	I/O	Function
1	Power_in	Power	Operational power input (DC9V to 48V)
2	GND	Power	Operational power input (GND)

5.8. CON9 (Power Output)

CON9 is an external output power connector. It outputs power from the AC adapter or the Power over Ethernet. Output voltage is determined according to the supplied power voltage.

- When using an AC adapter, total consumption current of Armadillo-210 must be less than 800mA.

- When using Power over Ethernet, total power consumption of Armadillo-210 must be less than 12.95W. (Standard power consumption of the Armadillo-210 main body is approx. 1.2W).

- Depending on operational environments, the Armadillo-210 could not be operational even if it was used below maximum rating. Be careful about this when using the Armadillo-210.

Table 5-10 CON9 Signal Assignment

Pin#	Signal Name	I/O	Function
1	Power_out	Power	External output power (DC9V to 48V) * In Power over Ethernet mode: Approx. DC48V
2	GND	Power	External output power (GND)

5.9. D1/D2 (Status LED)

D1 (green LED) and D2 (red LED) are connected to the CPU (EP9307)'s GPIO (General Purpose I/O), which allow controlling LED status (the LED connected to the GPIO Port E will function as the status LED when EP9307's built-in ROM boots up).

Note: The GPIO signal to be connected to this LED differs depending on board revision. For information on how to identify board revision, refer to Section 9.1, How to Identify Board Revision.

[Rev.A, Rev.B]

- D1 (green LED) is connected to the EP9307's RDLED (Port E: 1) pin.
- D2 (red LED) is connected to the EP9307'd GRLED (Port E: 0) pin.

[Rev.C or later]

- D1 (green LED) is connected to the EP9307's GRLED (Port E: 0) pin.
- D2 (red LED) is connected to the EP9307's ROW7 (Port C: 7) pin.

Caution: The Rev.C or later boards use the EP9307's RDLED (PortE:1) in the internal circuit. Never change this setting.

5.10. JP1/JP2 - Boot Mode Selection Jumpers

JP1 and JP2 jumpers are used to select the boot mode on Armadillo-210.

5.10.1. JP1 - Boot ROM Selection Jumper

With JP1 shorted, the system will boot from the on-chip boot ROM. When JP1 is open, the system will instead load the boot program from the on-board flash memory.

5.10.2. JP2 – Bootloader Mode Selection Jumper

JP2 is used by Hermit-at, the standard bootloader on Armadillo-210. When JP2 is shorted, Hermit-at will start in interactive mode, displaying a prompt on the serial terminal and then waiting for user input. When JP2 is open, Hermit-at will directly load Linux without any need for user intervention.

Table 5-11 jumper Setting and Behavior

JP1	JP2	Behavior at Booting
Open	Open	The Linux Kernel in On-board Flash Memory will boot up.
Open	Short	The boot loader "Hermit" command prompt will boot up.
Short	-	The program in On-chip Boot ROM will boot up.

5.11. LAN Connector LED

The LED at the bottom of the LAN connector shows status of LAN.

Table 5-12 Status of a LAN Connector LED

LED	Name	ON	OFF
Green	LINK	A LAN cable is connected. A 10BASE-T or 100BASE-TX link is established.	A LAN cable is not connected or the device to which the LAN cable is connected is not active.
Yellow	LAN	Data is being transmitted/received.	No data is transmitted/received.

5.12. Structure of a Power Circuit

The structure of a power circuit in the Armadillo-210 is shown in Figure 5-3. Be careful not to exceed the current capacity limitation when connecting each external device.

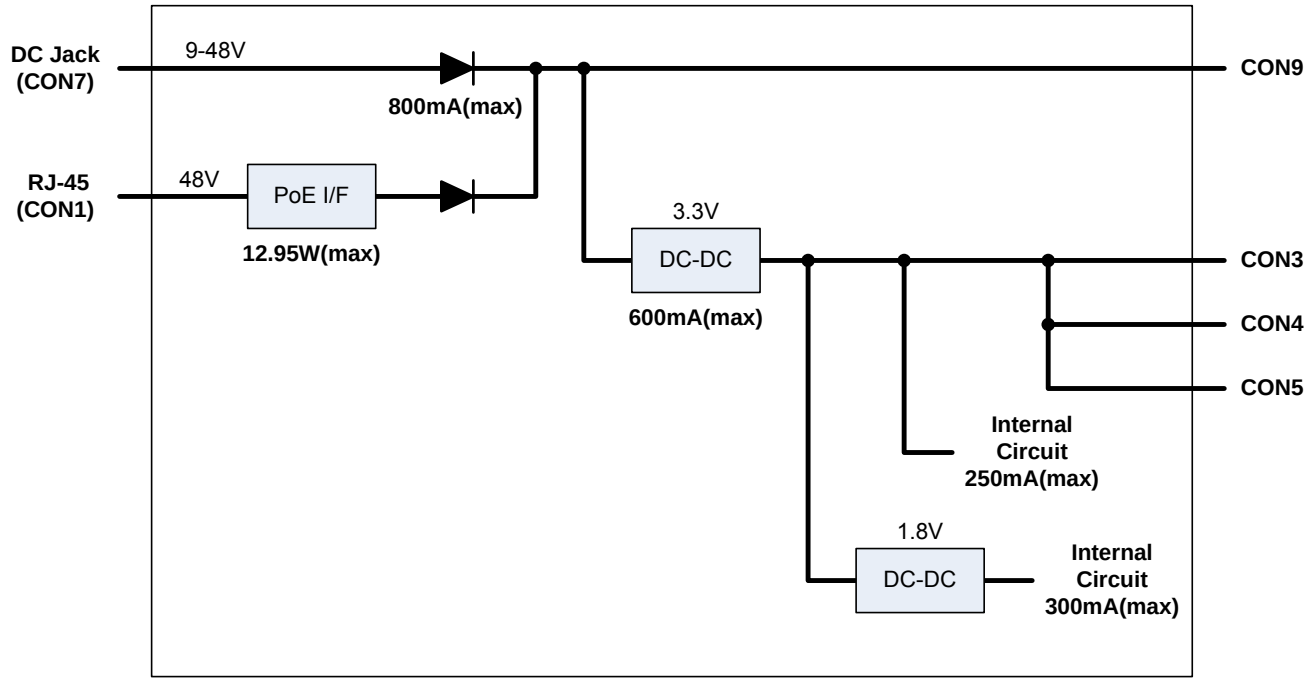


Figure 5-3 Structure of a Power Circuit in Armadillo-210

6. Example of a Reference Circuit

A reference circuit when using the CON5 (GPIO) is shown in Figure 6-1.

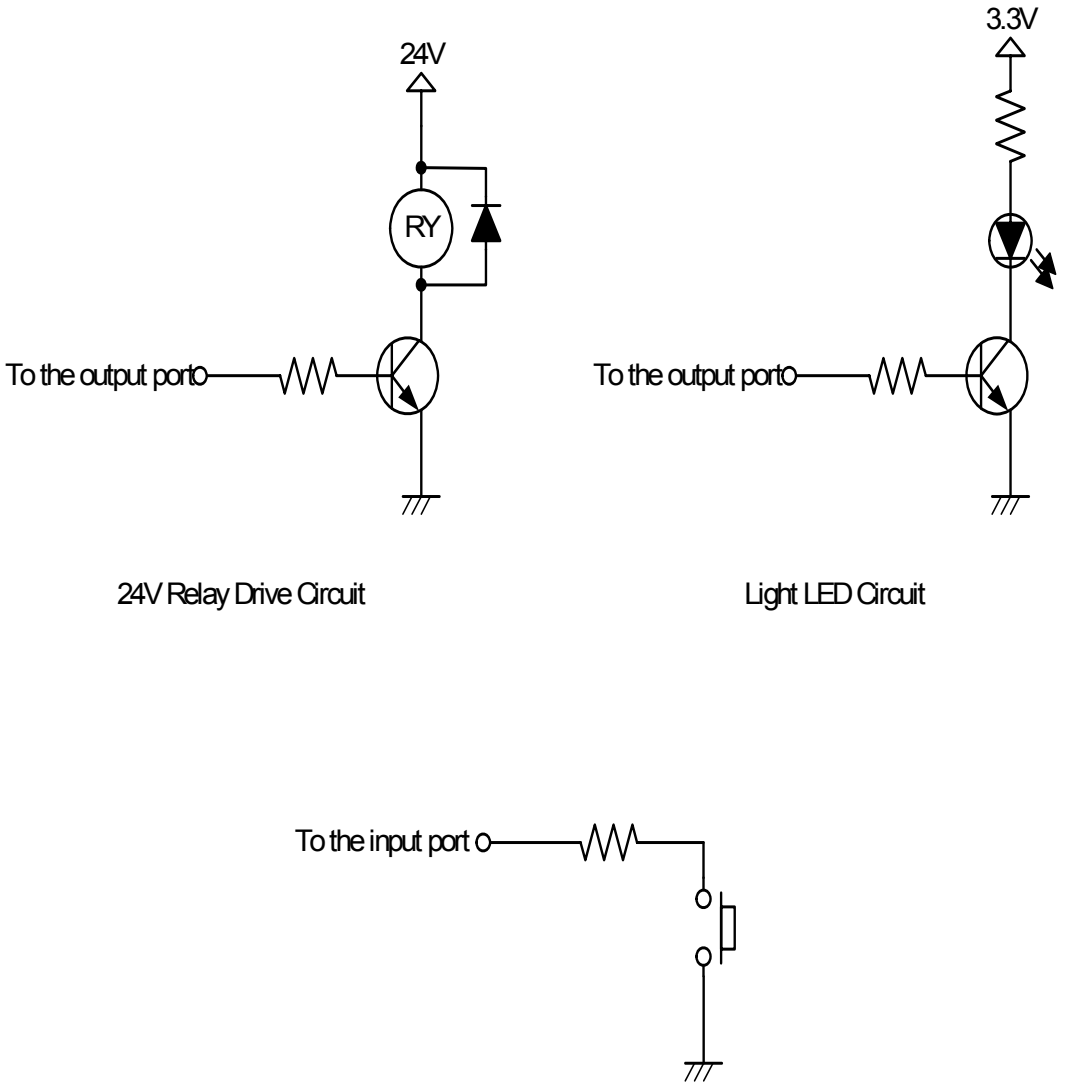
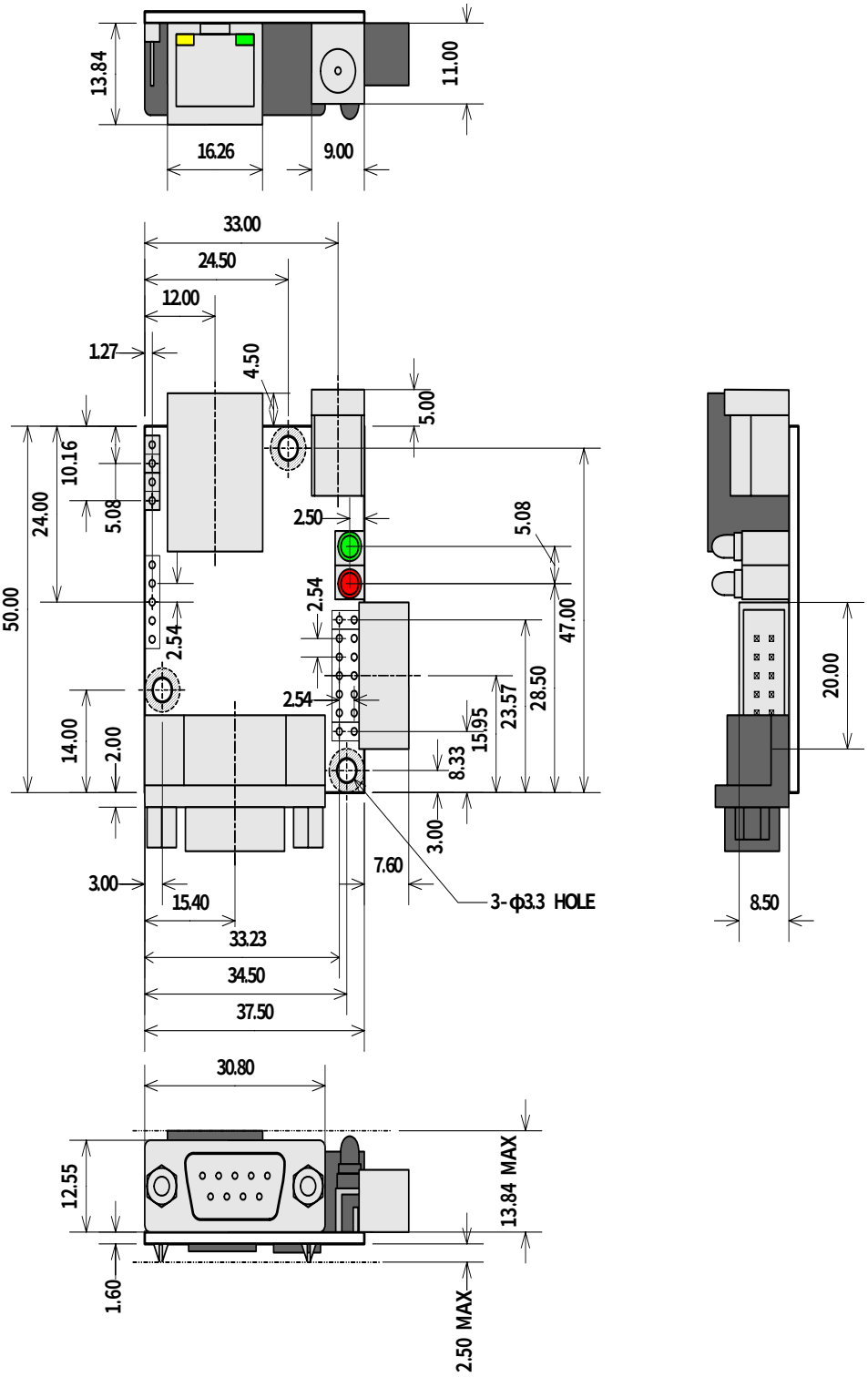


Figure 6-1 Example of a Reference Circuit

7. Board Layout

The layout of the Armadillo-210 board is shown in Figure 7-1.

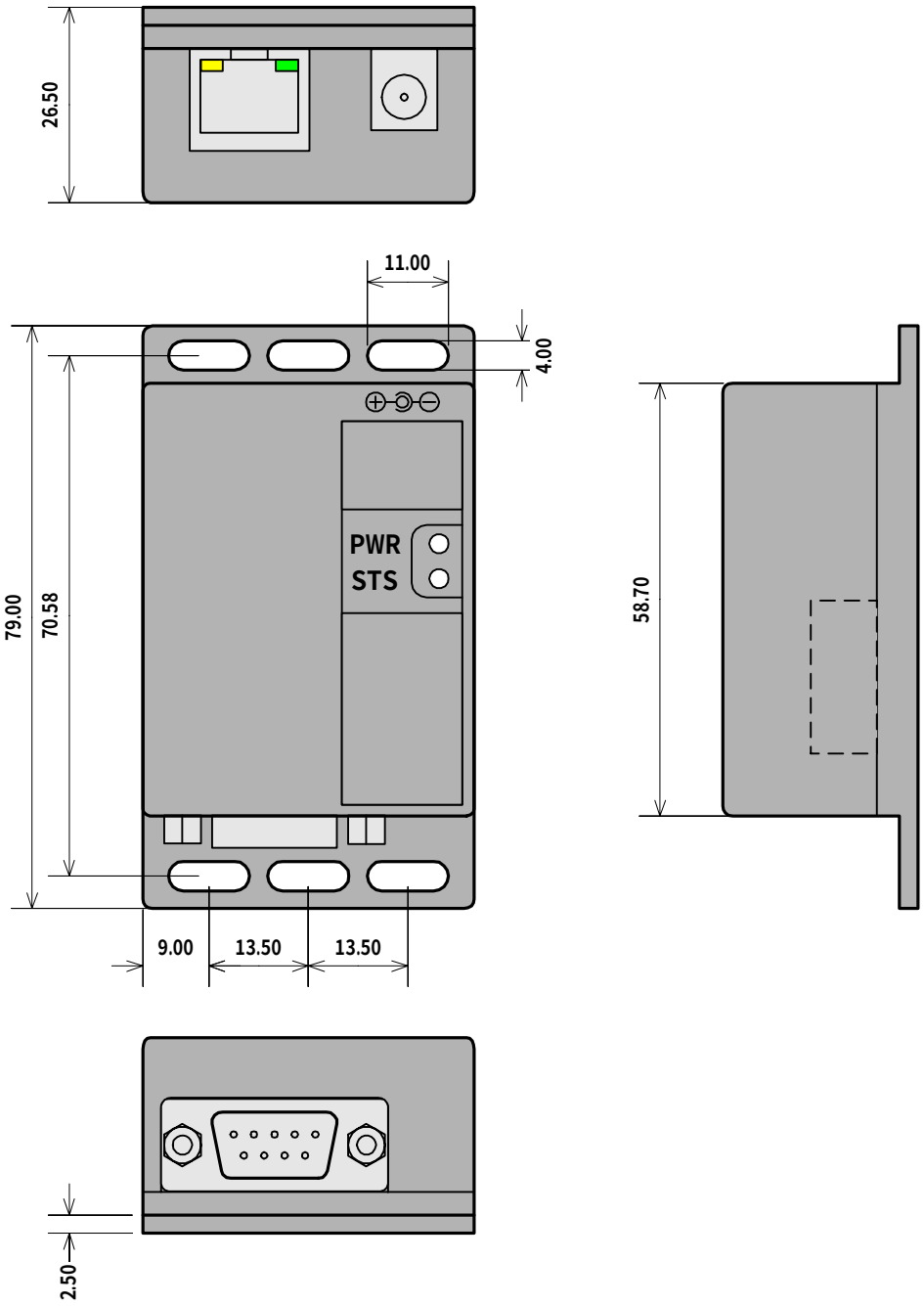


[Unit: mm]

Figure 7-1 Armadillo-210 Board Layout

8. Case Layout

The layout of the Armadillo-210 case is shown in Figure 8-1.



[Unit: mm]

Figure 8-1 Armadillo-210 Case Layout

9. Appendix

9.1. How to Identify Board Revision

The revision of the Armadillo-210 board is silk-printed at the position shown in Figure 9-1.

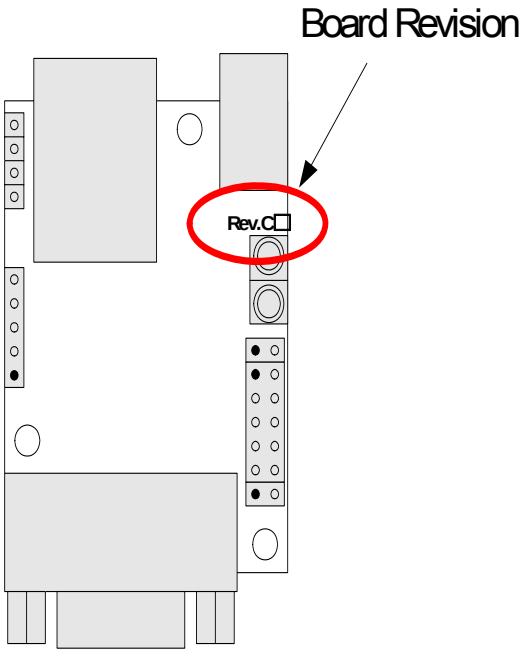


Figure 9-1 Armadillo-210 Board Revision

10. Revision History

Revision History

Ver.	Date	Revisions
1.0.0	2005.12.15	- Initial release
1.0.1	2006.8.11	- Added a description about output current in Table 5-4, Table 5-5 and Table 5-6. - Added Section 5.9, “D1/D2 (Status LED)”. - Added Section 5.12 “Structure of a Power Circuit”. - Added Section 9.1 “ How to Identify Board Revision”.

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